



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-6018A

Microwave End Product Board Inspection and Test

IPC-6018A

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A standard developed by IPC

Supersedes IPC-6018
January 1998

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IPC-6018A

Microwave End Product Board Inspection and Test

Developed by the High Speed/High Frequency Board Performance Subcommittee (D-22) of the High Speed/High Frequency Committee (D-20) of IPC

Supersedes:

IPC-6018 - January 1998

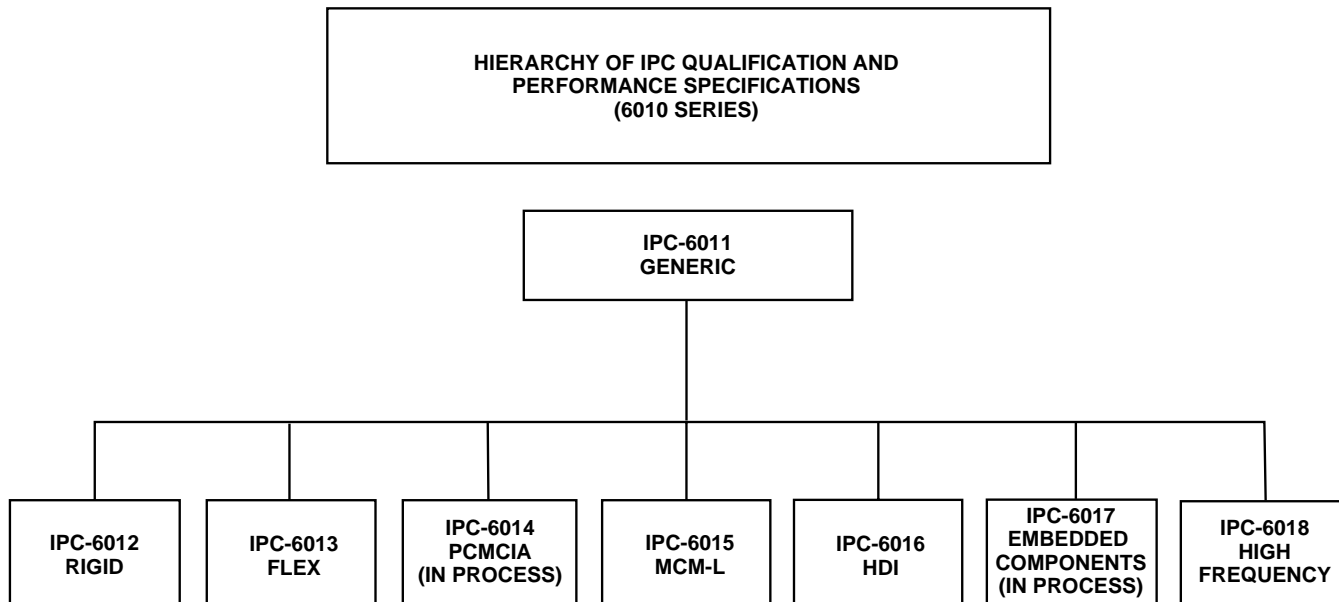
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Users of this standard are encouraged to participate in the development of future revisions.

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FOREWORD

This specification is intended to provide information on the detailed performance criteria of high frequency printed boards. It supersedes IPC-6018 and was developed as a revision to that document. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

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Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

Acknowledgment

Any standard involving a complex technology draws material from a vast number of sources. While the principal members of the High Speed/High Frequency Board Performance Subcommittee (D-22) of the High Speed/High Frequency Committee (D-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Microwave End Product Board Inspection and Test

1 SCOPE

1.1 Scope This specification covers end product inspection and test of high frequency (microwave) printed boards for microstrip, stripline, mixed dielectric and multilayer stripline applications with or without buried/blind vias, and metal cores.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of high frequency (microwave) printed wiring boards.

1.3 Performance Classification and Types

1.3.1 Classification This specification recognizes that the printed boards will be subject to variations in performance requirements based on end-use. The high frequency printed wiring boards are classified by Performance Class 1, 2, or 3. Performance classes are defined in IPC-6011, Generic Performance Specification for Printed Boards.

1.3.2 Board Type This specification will define seven types of high frequency (microwave) boards.

Type 1 — Single Sided

Type 2 — Double Sided

Type 3 — Homogeneous Multilayer Construction

Type 4 — Mixed Dielectric Multilayer

Type 5 — Homogeneous Multilayer with Blind and/or Buried Vias

Type 6 — Mixed Dielectric Multilayer with Blind and/or Buried Vias

Type 7 — Metal Core/Backed Boards

1.3.3 Selection for Procurement For procurement purposes, performance class **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is shown in IPC-D-325.

1.3.3.1 Selection The procurement documentation should specify the requirements that can be selected within this specification. Refer to Table 1-1 for a listing of default requirements.

1.3.4 Material, Plating Process and Final Finish

1.3.4.1 Laminate Material Laminate material is identified by numbers and/or letters, classes, types as specified by the appropriate specification listed in the procurement documentation.

Table 1-1 Default Requirements

Category	Default Selection
Performance Class	Class 2
Final Finish	Finish X (Electrodeposited tin-lead, fused or solder coated)
Minimum Starting Foil	1/2 oz. For all internal and external layers except for Type 1 which shall start with one ounce.
Copper foil type	Electrodeposited
Hole Diameter tolerances Plated, components Plated, via only Unplated	(±) 100 µm [3937 µin] (+) 80 µm [3150 µin], (-) no requirement, may be totally or partially plugged (±) 80 µm [3150 µin]
Conductor Width Deviation	Class 2 deviation per para. 3.6.2.1
Conductor Spacing Deviation	Class 2 deviation per para. 3.6.2.2
Marking Ink	Contrasting color, nonconductive
Solder Resist	Not applied if not specified
Solderability Test	Category 2 of J-STD-003
Solder Resist Specified	Class T of IPC-SM-840 if class not specified
Test Voltage Insulation Resistance	500 volts D.C., Class 2 per para. 3.11.7

1.3.4.2 Plating Process The copper plating process which is used to provide the main conductor in the holes is identified by one number as follows:

- 1 Acid copper electroplating only
- 2 Pyrophosphate copper electroplating only
- 3 Acid and/or pyrophosphate copper electroplating
- 4 Additive/electroless copper

1.3.4.3 Final Finish The final finish can be but is not limited to one of the finishes specified below or a combination of several platings and is dependent on assembly processes and end-use. Thickness, where required, **shall** be specified in the procurement documentation unless listed in Table 3-2. Coating thickness may be exempted in Table 3-2 (i.e., tin-lead plate or solder coating). Designators for final finish are as follows:

S	Solder Coating (Table 3-2)
T	Electrodeposited Tin-Lead, fused) (Table 3-2)
X	Either Type S or T (Table 3-2)
TLU	Electrodeposit Tin-Lead (unfused) (Table 3-2)
G	Gold Electroplate for Edge Board Connectors (Table 3-2)
GS	Gold Electroplate for Areas to be Soldered (Table 3-2)

N	Nickel for Edge Board Connectors (Table 3-2)
NB	Nickel as a Barrier to Copper-Tin Diffusion (Table 3-2)
OSP	Organic Solderability Protector (tarnish and solderability protection during storage and assembly processes) (Table 3-2)
C	Bare Copper (Table 3-2)
SMOBC	Solder Mask over Bare Copper
EN	Electroless Nickel
EG	Electroless Gold
IG	Immersion Gold
IS	Immersion Silver
IT	Immersion Tin
TN	Tin-Nickel
R	Rhodium
P	Palladium
TP	Tin Plating
Y	Other

1.4 Master Drawing Printed circuit boards furnished under this specification **shall** meet the design features detailed in IPC-D-316/IPC-2221 and the requirements of the approved master drawing. Type 4 and Type 6 boards will comply to IPC-D-316 for the RF Microwave portions and IPC-2221 for the mixed dielectric portions of the board. In the event of conflict between the design guides and the approved master drawing, the master drawing **shall** govern and a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Tolerances and dimensions not specified on the master drawing **shall** revert to those in this document.

2 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the date of contract agreement, form a part of this specification to the extent provided herein.

2.1 IPC¹

IPC-A-47 Composite Test Pattern Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-148A Resin Coated Metal Foil for Printed Boards

IPC-D-316 Design and Manufacturing Guide for RF/Microwave Circuit Boards

IPC-D-325 End Product Documentation for Printed Boards

IPC-A-600 Acceptability of Printed Boards

IPC-AI-642 User's Guidelines for Automated Inspection of Artwork, Innerlayers, and Unpopulated PWBs

IPC-TM-650 Test Methods Manual²

2.1.1 Microsectioning

2.1.1.2 Microsectioning—Semi or Automatic Technique
Microsection Equipment (Alternate)

2.1.9 Surface Scratch Examination Metal Clad Foil

2.2.10 Hole Location and Conductor Location

2.2.11 Registration, Terminal Pads

2.3.15 Purity, Copper Foil

2.3.25 Detection of Ionizable Surface Contamination
(Static Method)

2.3.26 Detection of Ionizable Surface Contamination
(Dynamic Method)

2.3.26.1 Resistivity of Solvent Extract

2.4.1 Adhesion, Plating

2.4.18 Tensile Strength and Elongation, Copper Foil

2.6.2.1 Water Absorption, Rigid Printed Wiring

2.6.3 Moisture and Insulation Resistance

2.6.7 Thermal Shock and Continuity (Flexible Printed
Wiring)

2.6.8 Thermal Stress, Plated-Through Holes

IPC-CC-830 Qualification and Performance of Electrical
Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent
Solder Mask

IPC-2141 Controlled Impedance Circuit Boards and High
Speed Logic Design

IPC-2221 Generic Design Standard for Printed Boards

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4101 Specification for Base Materials for Rigid and
Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High
Speed/High Frequency Applications

IPC-4203 Adhesive Coated Dielectric Films for Use as
Cover Sheets in Flexible Printed Wiring and Flexible
Bonding Films

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6011 Generic Performance Specification for Printed
Boards

1. IPC, 2215 Sanders Road, Northbrook, IL 60062

2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6015 Qualification and Performance Specification for Organic Multichip Modules (MCM-L) Mounting and Interconnecting Structures

IPC-9191 General Requirements for Implementation of Statistical Process Control (SPC)

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

J-STD-003 Solderability Test Methods for Printed Wiring Board

2.2 American Society for Testing and Materials³

ASTM-D-3165 Strength Properties of Adhesion in Shear By Tension Loading of Laminated Assemblies

ASTM-B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Use

ASTM-B-579 Standard Specification for Electrodeposited Coatings of Tin-Lead Alloy (Solder Plate)

2.3 Society of Automotive Engineers⁴

AMS-QQ-N-290 Nickel Plating (Electrodeposited)

3 REQUIREMENTS

3.1 Terms and Definitions Terms and definitions **shall** be in accordance with IPC-T-50, and as defined below.

White Spots Subsurface white or translucent spots occurring in woven glass PTFE at the glass knuckles after processing. This differs from measles and crazing in that the resin is not fractured.

Hybrid (Composite) Circuit Board Mixed dielectric multilayer printed circuit board.

3.2 General Printed boards furnished under this specification **shall** meet or exceed all the requirements of the specific performance class as required by the procurement documentation. Design features and coupon configuration **shall** be per IPC-2221 and IPC-D-316. Boards which must meet other special requirements beyond those specified in Section 3 will be as specified by the procurement document and/or the drawing.

Boards furnished under this specification **shall** be as specified by the master drawing. Unless otherwise specified, the finished printed circuit board **shall** meet the dimensional

requirements specified herein, on the master drawing and in accordance with IPC-2615. They **shall** be fabricated from panels that include sufficient coupons or production boards to perform the testing requirement of the class to which the boards were produced. Test coupons used to verify registration, plating integrity or impedance **shall** be arranged so that they are within 6 mm to 13 mm [0.24 in to 0.512 in] of the production board. Board apportionment to panels **shall** be such that coupons and location are representative of the board panel processing, and such that the location integrity of the coupons-to-board images **shall** be verified. Unless otherwise specified, the test coupons **shall** be identified by lot and/or by board serial number when the boards are serialized, and they **shall** be packaged with the appropriate board(s).

Boards furnished under this specification **shall** be processed in such a manner as to be uniform in quality and free from defects in excess of those allowed in this specification.

3.2.1 Master Drawing The master drawing **shall** be prepared in accordance with IPC-D-325. It **shall** establish the size and shape of the board, the size and location of all holes therein, and the shape or arrangement of both conductive and nonconductive patterns or elements. Any and all pattern features not controlled by the hole sizes and locations **shall** be dimensioned either specifically, or by notes. Dimensioning **shall** be in accordance with IPC-2615. When this specification is referenced on the master drawing, any exceptions or deviations **shall** be documented on that drawing.

3.3 Materials Used in this Specification

3.3.1 Laminates and Bonding Material for Multilayer or Mixed Dielectric Boards Rigid metal clad laminates, rigid unclad laminates and bonding material (prepreg or bonding film) should be selected from IPC-4101, IPC-4103, IPC-4203, or NEMA LI-1. The specification sheet number, metal cladding type and metal clad thickness (weight) **shall** be as specified in the procurement documentation. When specific requirements such as the flammability requirements shown in UL 94 for laminate and bonding materials are required, it is necessary to specify those requirements in material procurement documents. New materials can be called using IPC-4103.

3.3.1.1 Dielectric Layer Thickness The minimum and maximum dielectric layer thickness **shall** be as defined on the master drawing. Measurements **shall** be valley to valley (surface).

3. ASTM, 100 Barr Harbor Drive, West Conshohocken, PA 19428

4. SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001. www.sae.org

3.3.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners to the printed board **shall** be selected from IPC-4101, IPC-4103, IPC-4203 or as specified in the procurement documentation. New bonding materials can be called out per IPC-4103.

3.3.3 Other Dielectric Materials Photoimageable dielectrics should be selected from IPC-DD-135 and specified in the procurement documentation. Other dielectric materials may be specified in the procurement documentation.

3.3.4 Metal Foils Copper foil **shall** be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment and foil profile should be specified on the master drawing if critical to the function of the printed board. Resin coated copper foil **shall** be in accordance with IPC-CF-148. Resistive metal foil **shall** be in accordance with the applicable specification and the procurement documents.

3.3.5 Metal Core/Backed The metal core substrate **shall** be specified on the master drawing as shown in Table 3-1.

Table 3-1 Metal Core Substrate

Material	Specification	Alloy
Aluminum	QQ-A-250	As specified
Steel	QQ-S-635	As specified
Copper	ASTM-B 152 or IPC-4562	As specified
Copper-Invar Copper	IPC-CF-152	As specified
Copper-Moly-Copper	IPC-CF-152	As specified
Brass	SAE AMS 4505	As specified
Other	As specified	

3.3.6 Metallic Platings and Coatings Thickness of the plating/coating **shall** be in accordance with Table 3-2. The copper plating thickness on the surface, in plated-through holes, via holes and in blind and/or buried vias **shall** be as specified in Table 3-2. Thickness of platings for a specific use is shown in Table 3-2. Final finishes selected from those listed in 1.3.4.3 or combinations required **shall** specify plating thickness except for fused tin-lead plating or solder coating which requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges; conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.6.3.10. Electronic thickness measurements can be used for Class 1 and 2 boards.

Note: The Category of solderability testing **shall** be specified by the user per J-STD-003; however, in the event it is not specified the supplier **shall** test to Category 2 (steam aging is not required).

3.3.6.1 Electroless Depositions and Conductive Coatings Electroless depositions and conductive coatings

shall be sufficient for subsequent plating process and may be either electroless metal, vacuum deposited metal, or metallic or nonmetallic conductive coatings.

3.3.6.2 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

3.3.6.3 Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-2 applies.

3.3.6.4 Solder Coating The solder used for solder coating **shall** be Sn60A, Sn60C, Pb40A, Pb36A, Pb36B, Pb36C, Sn63A, Sn63C or Pb37A per J-STD-006.

3.3.6.5 Nickel Nickel plating **shall** be in accordance with AMS-QQ-N-290 Class 2, except the thickness **shall** be in accordance with Table 3-2.

3.3.6.6 Gold Plating Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Class and Type **shall** be specified in the procurement documentation. For Class 3 boards, gold plating **shall** be Type 1 or 3, Class 1.

Gold plating thickness on areas to be wire bonded **shall** be as specified in the procurement documentation (see IPC-6015, for example).

3.3.6.7 Other Other depositions such as bare copper, electroless nickel, immersion gold, immersion silver, palladium, rhodium, tin, 95Sn/5Pb etc. may be used provided they are specified in the procurement documentation.

3.3.6.8 Electrodeposited Copper When specified, electrodeposited copper **shall** meet the following criteria. Frequency of testing **shall** be determined by the manufacturer to ensure compliance.

- When tested as specified in IPC-TM-650, Method 2.3.15, the purity of the copper **shall** be no less than 99.50% for either pyrophosphate or acid copper.
- When tested as specified in IPC-TM-650, Method 2.4.18.1, ambient using 50 - 100 μm [1969 μin - 3937 μin] thick sample, the tensile strength **shall** be no less than 36,000 PSI [248 MPa] and the elongation **shall** be no less than 12%.

3.3.7 Organic Solderability Preservative (OSP) OSPs are anti-tarnish and solderability protectors applied to bare copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. Specific solderability retention

Table 3-2 Final Finish, Surface Plating Coating Requirements

Finish	Class 1	Class 2	Class 3
Gold (min) for edge-board Connectors and areas not to be soldered (electrolytic)	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
Gold (max) on areas to be soldered (electrolytic)	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]
Gold (Immersion)	0.1 µm [3.94 µin] min. 0.4 µm [15.7 µin] max	0.1 µm [3.94 µin] min. 0.4 µm [15.7 µin] max	0.1 µm [3.94 µin] min. 0.4 µin [15.7 µin] max
Nickel (min) for edge board connectors	2 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
Nickel (min) barrier to prevent formation of copper-tin compounds	1 µm [39.4 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
Unfused tin lead (min)	8 µm [315 µin]	8 µm [315 µin]	8 µm [315 µin]
Fused tin lead or solder coat	Coverage and solderable	Coverage and solderable	Coverage and solderable
Solder coat over bare copper	Coverage and solderable	Coverage and solderable	Coverage and solderable
Organic Solderability Preservative	Solderable	Solderable	Solderable
Bare Copper	None	None	None
Surface and Holes			
Copper ¹ (min average)	20 µm [787 µin]	25 µm [984 µin]	25 µm [984 µin]
Min thin areas ³	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Blind Via			
Copper ¹ (min average)	20 µm [787 µin]	25 µm [984 µin]	25 µm [984 µin]
Min thin areas ³	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Low Aspect Ratio		Blind Vias⁴	
Copper ¹ (min average)	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Min thin areas ³	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Buried Vias			
Copper ¹ (min average)	13 µm [512 µin]	13 µm [512 µin]	15 µm [592 µin]
Min thin areas ³	11 µm [433 µin]	11 µm [433 µin]	13 µm [512 µin]

1. Copper plating thickness applies to surface and hole walls

2. Nickel platings used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

3. For Class 3 boards having drilled hole diameter <0.35 mm [0.0138 in] and having aspect ratio >3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm [984 µin].

4. Low Aspect Ratio Blind Vias refer to blind vias produced using a controlled depth mechanism (e.g., laser, mechanical, plasma or photo defined) and having an aspect ratio of <2:1.

requirement, if applicable, **shall** be specified in the procurement documentation.

3.3.8 Polymer Coating (Solder Resist) When permanent solder resist coating is specified, it **shall** be a polymer coating conforming to IPC-SM-840.

3.3.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning the tin-lead plating and bare copper to allow for a smooth adherent coating. The fusing fluid **shall** act as a heat transfer and distribution media to prevent damage to the bare laminate of the board.

Note: Fusing fluid compatibility should be confirmed with end users' cleanliness requirements due to the diverse interactions experienced at assembly soldering.

3.3.10 Marking Inks Marking inks should not be used on PTFE surfaces. Marking inks **shall** be permanent, nonnutrient polymer inks, and **shall** be specified in the procurement documentation. Marking inks **shall** be applied to the board, or to a label applied to the board. Marking inks and labels must be capable of withstanding fluxes, cleaning solvents, soldering, cleaning and coating processes. If a conductive marking ink is used, the marking **shall** be treated as a conductive element on the board.

3.3.11 Hole Fill Insulation Material Electrical insulation material used for hole-fill for metal core printed boards or vias **shall** be as specified in the procurement documentation.

3.3.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes and bonding material **shall** be as specified in the procurement documentation.

3.4 Visual The boards **shall** be examined to verify that the design, construction, physical dimensions, markings, and workmanship are in accordance with the requirements outlined in this specification, and those defined on the printed board master drawing.

Visual inspection **shall** be at 7X to 30X magnification. Microvia magnification **shall** be at 30X, and critical dimensional requirements **shall** be measured at 30X to 100X.

3.4.1 Edges of Microwave Boards Burrs, nicks, and haloing along the edges of microwave boards **shall** be acceptable provided the penetration does not reduce the edge to conductor spacing more than minimum spacing specified on the master drawing. If no requirement is specified on the master drawing, the penetration **shall not** exceed 2.5 mm [0.0984 in]. Edge plating on microwave boards **shall** be defined on the master drawing. The master drawing **shall** define exceptions such as utilizing a ribbon of copper to connect upper and lower ground planes.

3.4.2 Laminate Imperfections Measling, crazing, blistering, delamination, and haloing **shall** be in accordance with IPC-A-600. Laminate defects **shall** be measured at 7X to 30X magnification, unless a magnification is previously agreed upon between user and supplier. Referee and critical measurement magnification for board features **shall** be 30X to 100X maximum.

3.4.2.1 Subsurface Imperfections Delamination is unacceptable. Subsurface imperfections such as haloing, foreign inclusions, variations in color and white or black spots **shall** be acceptable. The following additional requirement applies:

- a. No more than 1% of the board area on each side **shall** be affected. Reference IPC-A-600 for defect definitions.

3.4.2.2 Surface Appearance There **shall** be no resin starved or scorched areas, reinforcement exposure, foreign materials, blistering, or other visual defects detrimental to the performance of the laminate. Localized concentrations of these defects may occur, but they **shall** be no closer than 6.4 mm [0.252 in] to any conductor. The classification of the above defects **shall** be in accordance with IPC-A-600. Reinforcement texture and reinforcement areas exposed by mechanical fabrication operations are acceptable.

3.4.2.3 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable provided they do not bridge conductors or expose/disrupt fibers greater than allowed in the paragraphs above and do not reduce the dielectric spacing below the minimum specified.

3.4.2.4 Surface Voids Surface voids are acceptable provided they do not: exceed 0.8 mm [0.031 in] in the longest

dimension; bridge conductors; exceed 5% of the total board area; affect performance of the laminate.

3.4.2.5 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall not** exceed 10% of the total conductor surface area of the affected layer.

3.4.3 Plating and Coating Voids in the Hole Plating and coating voids **shall not** exceed that allowed by Table 3-3.

Table 3-3 Plating and Coating Voids Visual Examination

Material	Class 1	Class 2	Class 3
Copper	Three voids allowed per hole in not more than 10% of the holes	One void allowed per hole in not more than 5% of the holes	None
Finish Coating	Five voids allowed per hole in not more than 15% of the holes	Three voids allowed per hole in not more than 5% of the holes	One void allowed per hole in not more than 5% of the holes

Note 1: For Class 1 and 2 product, copper voids **shall not** exceed 5% of the hole length. Voids **shall not** extend beyond 90° of the circumference.

Note 2: For Class 2 and 3 product, finished coating voids **shall not** exceed 5% of the hole length. For Class 1, finished coating voids **shall not** exceed 10% of the hole length. Voids **shall not** extend beyond 90° for Class 1, 2 or 3.

3.4.4 Lifted Lands When visually examined in accordance with 3.4, the finished board **shall not** exhibit any lifted lands.

3.4.5 Marking Each individual board, each qualification board, and quality conformance test circuitry (as opposed to each individual test coupon) **shall** be marked in order to insure traceability between the boards/quality conformance test circuitry and the manufacturing history and to identify the supplier (logo, etc.). The marking **shall** be produced by the same process used in producing the conductive pattern, or by use of a permanent fungistatic ink or paint (on non-PTFE laminate see 3.3.10), LASER marker or by vibrating pencil marking on a metallic area provided for marking purposes or a permanently attached label. Conductive markings, either etched copper or conductive ink (see 3.3.10) **shall** be considered as electrical elements of the circuit and **shall not** reduce the electrical spacing requirements. All markings **shall** be compatible with materials and parts, legible for all tests, and in no case affect board performance. Marking **shall not** cover areas of lands that are to be soldered. Refer to IPC-A-600 for legibility requirements. In addition to this marking, the use of bar code marking is permissible. When used, date code **shall** be formatted per the supplier's discretion in order to establish traceability as to when the manufacturing operations were performed.

3.4.6 Solderability Only those printed boards that require soldering in a subsequent assembly operation require solderability testing. Boards that do not require soldering do not require solderability testing and this **shall** be specified on the master drawing, as in the case where press-fit components are used. Boards to be used only for surface mount do not require hole solderability testing. When required by the procurement documentation, accelerated aging for coating durability **shall** be in accordance with J-STD-003. The Category of durability **shall** be specified on the master drawing; however, if not specified, Category 2 **shall** be used. Test coupons or production boards to be tested **shall** be conditioned, if required, and evaluated for surface and hole solderability using J-STD-003.

When solderability testing is required, consideration should be given to board thickness and copper thickness. As both increase, the amount of time to properly wet the sides of the holes and the tops of the lands increases proportionately.

Note: Accelerated aging (steam aging) is intended for use on coatings of tin/lead, tin/lead solder or tin, but not other final finishes.

3.4.7 Plating Adhesion Printed boards **shall** be tested in accordance with the following procedure. The adhesion of the plating **shall** be tested in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape applied to the surface and removed by manual force applied perpendicular to the circuit pattern.

There **shall** be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal (slivers) breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of plating adhesion failure.

3.4.8 Edge Board Contact, Junction of Gold Plate to Solder Finish Exposed copper/plating overlap between the solder finish and gold plate **shall** meet the requirements of Table 3-4. The exposed copper/plating or gold overlap may exhibit a discolored or gray-black area which is acceptable (see 3.6.3.7).

Table 3-4 Edge Board Contact Gap

	Max. Exposed Copper Gap	Max. Gold Overlap
Class 1	2.5 mm [0.0984 in]	2.5 mm [0.0984 in]
Class 2	1.25 mm [0.04921 in]	1.25 mm [0.04921 in]
Class 3	0.8 mm [0.0315 in]	0.8 mm [0.0315 in]

3.4.9 Workmanship Printed boards **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, tin/

lead or solder smear transfer to the dielectric surface, flux residue and other contaminants that affect life, ability to assemble and serviceability. Visually dark appearances in nonplated holes, which are seen when a metallic or nonmetallic semiconductive coating is used, are not foreign material and do not affect life or function. Printed boards **shall** be free of defects in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the printed board.

3.4.9.1 Adhesive Bleed Out On type 3, 4, 5 and 6 boards, adhesive bleed out may occur. Conductors that are exposed by access holes or cutouts **shall** be free of adhesive, with the exception of a 0.75 mm [0.0295 in] maximum wide band at the junction of the conductor and the layer (see Figure 3-1). All adhesive in holes and cutouts **shall** be firmly bonded to the board surface. Unless otherwise defined on the master drawing, surface appearance **shall** meet the requirements of 3.4.2.2 (surface appearance).

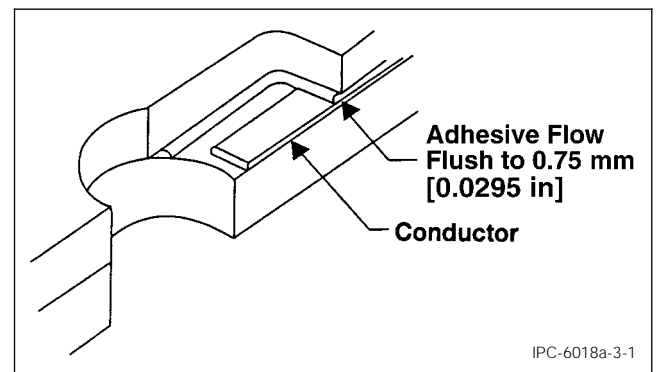


Figure 3-1 Adhesive Band Near Exposed Conductor

3.5 Board Dimensional Requirements The board **shall** meet the dimensional requirements specified in the procurement documents. Features of the board **shall** be measured at 7X to 30X magnification, unless a magnification is previously agreed upon between user and vendor.

Referee and critical measurement magnification for board features **shall** be 30X to 100X maximum. Conductor pattern **shall** be measured at 30X magnification with direct lighting across the gap width.

Automated inspection technology is allowed (see IPC-AI-642).

3.5.1 Hole Size, Slots and Hole Pattern Accuracy The hole size tolerance, slot tolerance and hole pattern accuracy **shall** be as specified in the procurement documentation. Nodules or rough plating in plated-through holes **shall not** reduce the hole diameter below the minimum limits defined

in the procurement document. Side walls or bottom surfaces **shall not** show any protrusions, rough edges, or burrs which decrease the usable area by more than the total profile tolerance defined by the master drawing.

3.5.2 Annular Ring and Breakout (Internal) The minimum internal annular ring **shall** meet the requirements of Table 3-5. Measurements for internal annular ring is from the inside of the drilled hole to the edge of the internal land as shown in Figure 3-2. Negative etchback is evaluated per 3.7.2.5. External pads of sequentially laminated structures are considered as an external layer and are evaluated in process prior to additional lamination(s) (see 3.5.3). Micro-section analysis is performed per 3.7.2 (see Figures 3-3A and 3-3B).

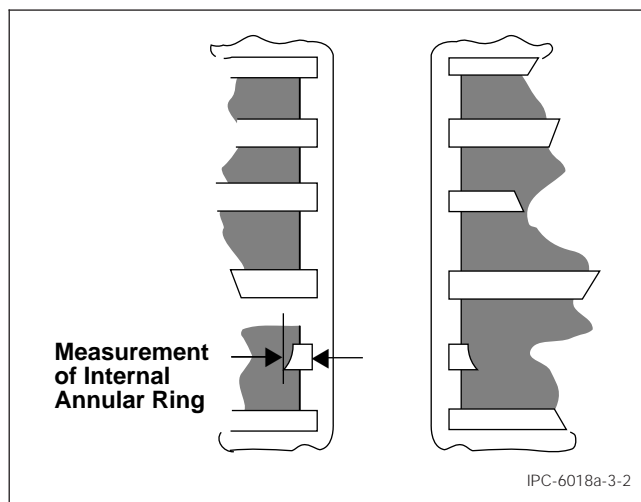


Figure 3-2 Annular Ring Measurement

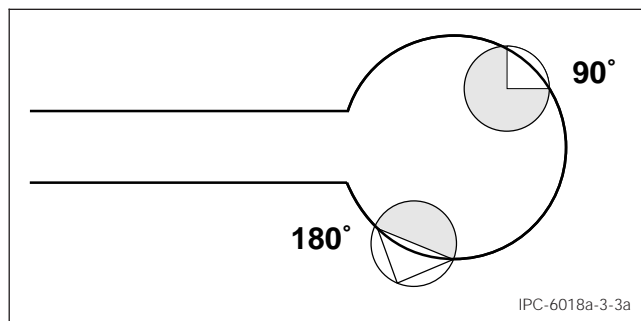


Figure 3-3a Breakout of 90° and 180°

Internal registration may be assessed by nondestructive techniques other than microsection, such as, special patterns, probes, and/or software which are configured to provide information on the interpolated annular ring remaining and pattern skew. Techniques include, but are not limited to the following:

- The optional F coupon (see 12.4.5 of IPC-2221 for F coupon design).
- Custom designed electrically testable coupons.

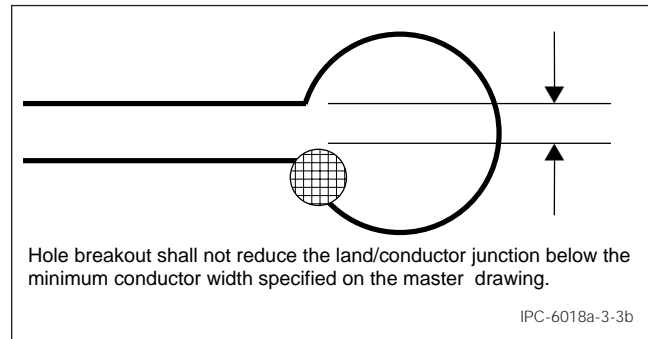


Figure 3-3b Conductor Width Reduction

- Radiographic (x-ray) techniques.
- Horizontal microsection.
- CAD/CAM data analysis as correlated to pattern skew by layer.

Note: It is recommended that microsectioning or statistical sampling is used to verify correlation of the approved technique, and a calibration standard is established for the specific technique employed.

3.5.3 Annular Ring (External) The minimum external annular ring shall meet the requirements of Table 3-5. The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole, or unsupported hole, to the outer edge of the annular ring on the surface of the board. For Class 2, plated-through holes identified as vias (not having a component) can have up to 90° breakout of the annular ring, and up to 180° breakout for Class 1. The break out **shall not** occur at the conductor/land intersection and the hole **shall** meet the requirements of 3.7.2.1 and 3.7.2.2. The finished board with the related breakout **shall** meet the electrical requirements of 3.10 (see Figures 3-3A and 3-3B).

3.5.4 Bow and Twist Unless otherwise specified in the procurement documentation, when designed in accordance with 5.2.4 of IPC-2221, the printed board shall have a maximum bow and twist of 0.75% for boards that use surface mount components and a maximum bow and twist of 1.5% for all other boards. Panels which contain multiple printed boards which are assembled on the panel and later separated shall be assessed in panel form

Bow, twist, or any combination thereof, **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22, which describes four procedures to determine bow and twist of either cut to size panels or finished rigid printed boards including single-sided, double-sided and multilayer.

3.6 Conductor Definition The conductor pattern **shall** have no tears or cracks, and **shall** conform to the design, construction, and physical dimensions defined on the master drawing. There **shall** be no delamination, blisters, or

Table 3-5 Minimum Annular Ring

Characteristic	Class 1	Class 2	Class 3
EXTERNAL Plated-through holes	Not greater than 180° breakout of hole from land when visually assessed. The land/conductor junction shall not be reduced below the allowable width reduction in 3.6.2.1.	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction shall not be reduced below the allowable width reduction in 3.6.2.1. The conductor junction should never be less than 50 μm [1969 μin] or the minimum line width, whichever is smaller.	The minimum annular ring shall not be less than 50 μm [1969 μin]. The land/conductor junction shall not be reduced below the minimum specified conductor width on the master drawing. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
INTERNAL Plated-through holes	Not greater than 180° breakout of hole from land. ¹ The land/conductor junction shall not be reduced below the allowable width reduction in 3.6.2.1.	Not greater than 90° breakout of hole from land. ¹ The land/conductor junction shall not be reduced below the allowable width reduction in 3.6.2.1. The conductor junction should never be less than 50 μm [1969 μin] or the minimum line width, whichever is smaller.	The minimum functional internal annular ring shall not be less than 25 μm [984 μin].
EXTERNAL Unsupported holes	No breakout at conductor junction.	No breakout allowed.	The minimum annular ring shall not be less than 150 μm [5906 μin]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

¹Minimum lateral spacing shall be maintained.

Note: (see Figure 3-3A and 3-3B for land breakout and conductor width reduction at land).

wrinkles in the conductive pattern. Edge definition includes any departure of the conductor edge from a smooth or straight contour. The edge of the conductor is defined by the outer-most edge of the metal. Edge irregularities determine the conductor width. Edge definition will be controlled by conductor width limits. The conductor line width is defined as the distance between the conductor edges. See Figure 3-4.

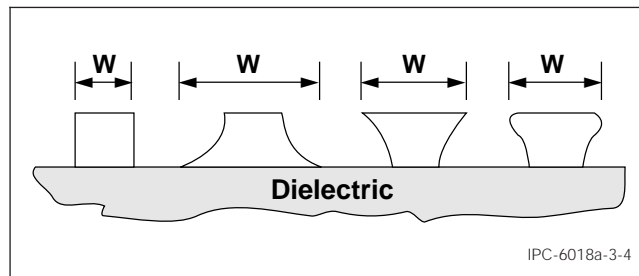


Figure 3-4 Conductor Edge Definition

Features of the board **shall** be measured at 7X to 30X magnification, unless a magnification is previously agreed upon between user and supplier. Referee and critical measurement magnification for board features **shall** be 30X to 100X maximum. Conductor pattern **shall** be measured at 30X magnification with direct lighting across the gap width.

3.6.1 Undercutting When determined by microsection (see 3.7), undercutting of the edge of the conductor **shall not** exceed the total thickness of clad and plated copper, or 10% of the conductor width, whichever is least (see Figure 3-5).

3.6.2 Conductor Width and Spacing Conductor width and spacing **shall** meet the requirements listed in 3.6.2.1 and 3.6.2.2.

Noncritical circuits and spacing **shall** have a tolerance of ± 0.075 mm [0.00295 in] unless otherwise specified on the master drawing.

Features of the board **shall** be measured at 7X-30X magnification, unless a magnification is previously agreed upon

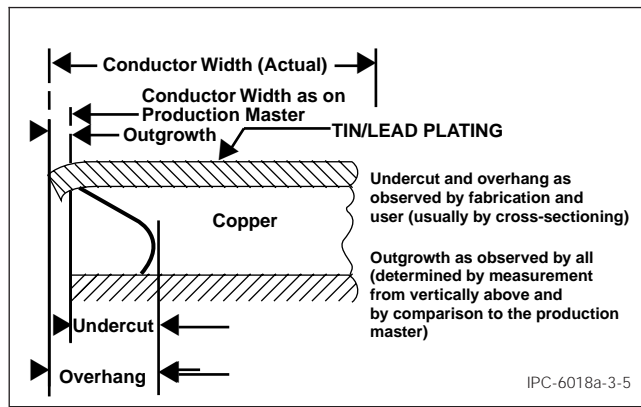


Figure 3-5 Undercut and Growth

between user and vendor. Referee and critical measurement magnification for board features **shall** be 30X to 100X maximum. Conductor pattern **shall** be measured at 30X magnification with direct lighting across the gap width.

3.6.2.1 Conductor Width A single deviation along any 25 mm [0.984 in] segment of a conductive pattern width specified on the master drawing **shall** be acceptable. Deviations on direct opposite sides of a conductor **shall not** exceed the total requirement when combined. Reference Table 3-6 for requirements. The maximum length of deviation **shall** be the same as the allowed width deviation.

Table 3-6 Percent of Allowable Conductor Width Deviations

Class 1	Class 2	Class 3
20%	10%	10%

3.6.2.2 Conductor Spacing Circuit spacing **shall** be defined on the master drawing, and **shall** be categorized as critical when required.

Isolated protrusions on multiple conductor boards **shall not** exceed the allowable limits defined in Table 3-7 when inspected to the requirements on the master drawing. Protrusions in proximity of, or directly opposite to, other protrusions **shall not** exceed the referenced limits in Table 3-7. The maximum length of protrusions **shall** be the same as the allowed width change. Critical conduct dimensions for 1/2 ounce copper are in Table 3-8.

Note: A single such protrusion is allowed along any 25 mm [0.984 in] segment of the conductor pattern with width specified on the master drawing.

Table 3-7 Percent of Allowable Conductor Space Deviations

Class 1	Class 2	Class 3
20%	10%	10%

3.6.3 Conductive Surfaces The requirements of 3.6.3.1 through 3.6.3.5 pertain to signal carrying conductive surfaces, and to ground planes where specifically identified.

Table 3-8 Critical Conductor Tolerance Requirements for 1/2 Ounce Copper

Class 1	Class 2	Class 3
0.05 mm [0.002 in]	0.025 mm [0.001 in]	0.013 mm [0.0005 in]

Features of the board **shall** be measured at 7X-30X magnification, unless a magnification is previously agreed upon between user and vendor. Referee and critical measurement magnification for board features **shall** be 30X to 100X maximum. Conductor pattern **shall** be measured at 30X magnification with direct lighting across the gap width.

3.6.3.1 Scratches A scratch of any length or width is permissible on ground planes, provided the dielectric is not exposed. Scratches on conductive patterns may be of any length, but no deeper than 20% of the total conductor thickness.

Testing for scratches should be in accordance with IPC-TM-650, Method 2.1.9. Other suitable electronic means may be used.

3.6.3.2 Pits Pits in ground planes are acceptable as long as the base dielectric is not exposed, and they do not exceed 25% of the surface area. Any pit in the conductive pattern is acceptable provided the dielectric substrate is not exposed and the outline dimension does not exceed 10% of the conductor width, and there is no more than one pit per 25 mm [0.984 in] of the conductor length.

3.6.3.3 Dents A dent of any length or width is permissible on ground planes, provided the clad surface is not torn. Dents on conductive patterns may be of any length, but no deeper than 0.013 mm [0.0005 in].

3.6.3.4 Pin Holes Pin holes on ground planes in noncritical areas are acceptable, as long as they have no single diameter greater than 0.5 mm [0.020 in] and do not exceed three per 25 mm [0.984 in] diameter. A pin hole in a conductive pattern is acceptable, provided the maximum dimension does not exceed the percent allowances in Table 3-9. Pin holes **shall** be limited to no more than one per 25 mm [0.984 in] of conductive length.

Table 3-9 Percent of Allowable Conductor Width Reduction Caused By Pin Holes

Class 1	Class 2	Class 3
20%	10%	10%

3.6.3.5 Superfluous Metal In general, small particles of metal such as residual copper or subsequent plating after etching which remain affixed to areas that are intended to be free of conductive material, while not desirable, **shall not** be cause for rejection unless: (1) they occur closer than 6.4 mm [0.252 in] to any conductor, or (2) they are larger

than 0.13 mm [0.00512 in] at their greatest diameter. Removal of superfluous metal is permissible, (1) as long as the surface appearance is not disturbed any deeper than that specified in Table 3-10, or (2) as long as the surface appearance is not disturbed any deeper than 10% of the board material thickness, whichever is less, on nonreinforced plastic sheet material, or (3) as long as there is no reinforcement exposure on reinforced plastic sheet material.

Table 3-10 Percent of Reduction in Dielectric Material Thickness

Class 1	Class 2	Class 3
20%	10%	10%

3.6.3.6 Surface Mount Lands Defects such as nicks, dents, and pin holes along the edge of the land **shall not** exceed 20% of either the length or width of the land for Class 2 or Class 3 boards, or 30% for Class 1. Defects internal to the land **shall not** exceed 10% of the length or width of the land for Class 2 or Class 3 boards, or 20% for Class 1.

3.6.3.7 Edge Board Connector Lands On gold or other noble metal plated edge board connector lands, except as noted below, the insertion or contact area **shall** be free of cuts or scratches that expose nickel or copper, solder splashes or tin-lead plating, and nodules or metal bumps that protrude above the surface. Pits, dents or depressions are acceptable if they do not exceed 0.15 mm [0.00591 in] in their longest dimension and there are not more than three per land and do not appear on more than 30% of the lands. The imperfection limits do not apply to a band 0.15 mm [0.00591 in] wide around the perimeter of the land including the insertion area.

3.6.3.8 Dewetting Dewetting on conductors, areas of solder connection, and ground or voltage planes is allowed to the extent listed below:

- a. Conductors and planes—permitted for all classes.
- b. Individual areas of solder connection:
 - Class 1 – 15%
 - Class 2 – 5%
 - Class 3 – 5%

3.6.3.9 Nonwetting For tin, tin/lead reflowed or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required.

3.6.3.10 Final Finish Coverage Final finish **shall** meet the solderability requirements of J-STD-003. Exposed copper on areas not to be soldered is permitted on 1% of the conductor surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor edges.

3.7 Structural Integrity Printed boards **shall** meet structural integrity requirements for thermally stressed (after solder float) evaluation test coupons specified in 3.7.2. Although the A and B coupons are assigned for this test, production boards may be used in lieu of the A/B coupons and are preferred for product that contains surface mount and vias or surface mount mixed with through-hole technology. Holes selected **shall** be equivalent to those specified for test coupons. The production boards and all other test coupons in the quality conformance test circuitry, which contain plated through-holes, **shall** be capable of meeting the requirements of this section. Structural integrity **shall** be used to evaluate test coupons or production boards from Type 2 through Type 6 boards by microsectioning techniques. Characteristics not applicable to Type 2 boards (i.e., requirements for innerlayer separations, innerlayer inclusions, and inner foil cracks) are not evaluated. Dimensional measurements that are only possible through the use of microsectioning techniques are also defined in this section. Blind and buried vias **shall** meet the requirements of plated-through holes.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed test coupon and all requirements must be met; however, per supplier election, certain properties and conditions as defined in the following paragraph(s), which are not affected by thermal stressing, may be evaluated in a test coupon(s) that has not been thermally stressed.

- a. When a supplier elects to evaluate the unstressed test coupon for the properties listed in (b), he may do so at any operation following the copper plating operation. If the board undergoes additional thermal excursions above the T_g (glass transition temperature) after copper plating, the unstressed test coupon being evaluated **shall** also be subjected to these thermal excursions.
- b. The properties which are not affected by thermal stress are: copper voids, plating folds/inclusions, burrs and nodules, glass fiber protrusion, wicking, final coating plating voids, etchback, negative etchback, plating/coating thickness, internal and surface copper layer or foil thickness.

3.7.1 Thermal Stress Testing Test coupons or production boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.8.

Following stress, test coupons or production boards **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1, or 2.1.1.2 on test coupons or production boards. A minimum of three holes or vias **shall** be inspected in the vertical cross section. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the three holes is within 10% of the drilled diameter of the hole.

Plated-through holes **shall** be examined for foil and plating integrity at a magnification of $100X \pm 5\%$. Referee examinations **shall** be accomplished at a magnification of $200X \pm 5\%$. Each side of the hole **shall** be examined independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination and plating voids, and so forth, **shall** be accomplished at magnifications specified above. Plating thicknesses below $1 \mu\text{m}$ [$39.4 \mu\text{in}$] **shall not** be measured using metallographic techniques.

Note: When agreed by user and supplier, alternate techniques may be used to supplement microsection evaluation.

3.7.2 Requirements for Microsectioned Coupons or Production Boards When examined in microsection, the test coupons or production boards **shall** meet the requirements of Table 3-11 and 3.7.2.1 through 3.7.2.17.

3.7.2.1 Plating Integrity Plating integrity in the plated-through holes **shall** meet the requirements detailed in Table 3-11. For Class 2 and 3 product, there **shall** be no separation of plating layers (except as noted in Table 3-11), no plating cracks, and internal interconnections **shall** exhibit no separation or contamination between plated hole wall and internal layers.

Metal core or thermal planes, when used as electrically functional circuitry, **shall** meet the above requirements when made from copper; but those made from dissimilar metals may have small spots or pits at their junction with the hole wall plating. Those areas of contamination or inclusions **shall** neither exceed 50% of each side of the interconnection, nor occur in the interface of the copper cladding on the core and the copper plating in the hole wall when viewed in the microsection evaluation. When the metal core is an external pad-less layer, separation is not allowed.

3.7.2.2 Plating Voids Class 1 product **shall** meet the requirements for plating voids established in Table 3-11. For Class 2 and 3 product, there **shall** be no more than one void per test coupon or production board, and the following criteria must be met:

- There **shall** be no more than one plating void per test coupon or production board, regardless of length or size.
- There **shall** be no plating void in excess of 5% of the total printed wiring board thickness.
- There **shall** be no plating voids evident at the interface of an internal conductive layer and plated hole wall.
- Circumferential plating voids are not allowed.
- Pad-less through holes **shall not** have plating voids at external layers.

If a void is detected during evaluation of a microsection which meets the above criteria, resample in accordance

with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no plating voids, the product which the test coupon or production boards represent are considered acceptable; however, if a plating void is present in the microsections, the product **shall** be considered non-conforming.

3.7.2.3 Laminate Integrity For Class 2 and 3 products, there **shall** be no laminate voids in Zone B (Figure 3-6) in excess of $80 \mu\text{m}$ [$3150 \mu\text{in}$]. For Class 1 products, voids allowed in Zone B (Figure 3-6) **shall not** exceed $150 \mu\text{m}$ [$5906 \mu\text{in}$]. Multiple voids between two adjacent plated-through holes in the same plane **shall not** have a combined length which exceeds these limits. Delamination is not acceptable in Zones A and B.

3.7.2.4 Laminate Cracks Laminate cracks in Zone A (Figure 3-6) are acceptable. Cracks which originate in Zone A and extend into Zone B or are entirely in Zone B **shall not** be in excess of $80 \mu\text{m}$ [$3150 \mu\text{in}$] for Class 2 or 3 products, and $150 \mu\text{m}$ [$5906 \mu\text{in}$] for Class 1 products. Multiple cracks between two adjacent plated-through holes in the same plane **shall not** have a combined length which exceeds these limits. Cracks between two uncommon conductors in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.7.2.5 Etchback

3.7.2.5.1 Non-PTFE Laminates When specified (Type 4 and 6 boards) on the master drawing, printed boards **shall** be etched back for the lateral removal of resin and/or glass fibers from the drilled hole walls prior to plating. The etchback **shall** be between $5 \mu\text{m}$ [$197 \mu\text{in}$] and $80 \mu\text{m}$ [$3150 \mu\text{in}$] with a preferred depth of $13 \mu\text{m}$ [$512 \mu\text{in}$], unless in contact with a PTFE layer. A two point connection is permitted on one side of each land (Figure 3-7). When no etchback is specified and the board manufacturer elects to use etchback, the manufacturer **shall** be qualified to perform etchback in his qualification test coupons or boards.

Caution: Etchback greater than $50 \mu\text{m}$ [$1969 \mu\text{in}$] may cause folds or voids in the plating, which then may not meet the required copper thickness.

3.7.2.5.2 Etchback on PTFE Laminates Etchback **shall** be between a negative etchback of $25 \mu\text{m}$ [$984 \mu\text{in}$] and a positive etchback of $50 \mu\text{m}$ [$1969 \mu\text{in}$].

3.7.2.6 Smear Removal

3.7.2.6.1 Smear Removal on Non-PTFE Laminates Smear removal is removal of resin debris which results from the formation of the hole. Smear removal **shall** be

Table 3-11 Plated-Through Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper voids	Three voids allowed per hole. Voids in the same plane are not allowed. No void shall be longer than 5% of board thickness. No circumferential voids allowed.	One void allowed per specimen provided the additional microsection criteria of 3.7.2.2 are met.	One void allowed per specimen provided the additional microsection criteria of 3.7.2.2 are met.
Plating folds/inclusions ¹	Must be enclosed.	Must be enclosed.	Must be enclosed.
Burrs ² and nodules ¹	Allowed if minimum hole diameter is met.	Allowed if minimum hole diameter met.	Allowed if minimum hole diameter met.
Glass fiber protrusion	Allowed. See 3.7.2.10	Allowed. See 3.7.2.10	Allowed. See 3.7.2.10
Wicking	125 µm [4921 µin] maximum	100 µm [3937 µin] maximum	80 µm [3150 µin] maximum
Innerlayer inclusions (inclusions at the interface between internal lands and through-hole plating).	Allowed on only one side of hole wall at each land location on 20% of available lands	None allowed	None allowed
Internal foil cracks	“C” cracks allowed on only one side of hole provided it does not extend through foil thickness.	None allowed	None allowed
External foil cracks ¹ . (type “A”, “B” and “D” cracks)	“D” cracks not allowed. “A” and “B” cracks allowed.	“D” and “B” cracks not allowed. “A” cracks allowed.	“D” and “B” cracks not allowed. “A” cracks allowed.
Barrel/Corner cracks (type “E” and “F” cracks)	None allowed	None allowed	None allowed
Innerlayer separation (separation at the interface between internal lands and through-hole plating).	Allowed on only one side of hole wall at each land location on 20% of available lands.	None allowed	None allowed
Separations along the vertical edge of the external land(s)	Allowed (see Figure 3-10) provided it does not extend beyond the vertical edge of the external copper foil.		
Plating separation	Allowed at knee, maximum length 125 µm [4921 µin].	None allowed	None allowed
Hole wall dielectric/ plated barrel separation.	Acceptable provided dimensional and plating requirements are met.	Acceptable provided dimensional and plating requirements are met.	Acceptable provided dimensional and plating requirements are met.
Lifted lands after thermal stress or rework simulation.	Allowed provided the finished boards meet the visual criteria of 3.3.4.		

“A” crack = A crack in the external foil

“B” crack = A crack that does not completely break plating (minimum plating remains)

“C” crack = A crack in the internal foil

“D” crack = A crack in the external foil and plating - complete break in foil and plating

“E” crack = A barrel crack in plating only

“F” crack = A corner crack in the plating only

¹The minimum copper thickness in Table 3-2 must be met.

sufficient to meet the acceptability criteria for plating separation (see Table 3-11). Smear removal **shall not** be etched back greater than 25 µm [984 µin]; random tears or drill gouges which produce small areas where the 25 µm [984 µin] in depth is exceeded **shall not** be evaluated as smear removal. Smear removal is not required of Type 1 or Type 2 boards.

3.7.2.6.2 Resin Smear on PTFE Laminates Allowable resin smear **shall** be 25% of the vertical inner layer requirement for Type 3 through 6 boards. There is no requirement for Type 1 or 2 boards. Resin removal (etchback) caused by smear removal **shall** meet the requirements of Table 3-11. Two or three point plating connection is not required. Referee testing **shall** be performed by hori-

zontal microsection. Smear extending around more than 33% of the circumference of the hole in question **shall** be rejectable.

3.7.2.7 Negative Etchback on Non-PTFE Laminates Negative etchback **shall not** exceed the requirements shown in Figure 3-8.

3.7.2.8 Microsection Annular Ring (Internal) Internal annular ring, if not determined by the techniques in 3.5.2, **shall** be measured by microsection to verify conformance to Table 3-5 as shown in Figure 3-2. If internal annular ring breakout is detected in the vertical cross section but the degree of breakout can not be determined, it **shall** be measured by horizontal microsection. The test coupon or production board used for the horizontal microsection **shall** be

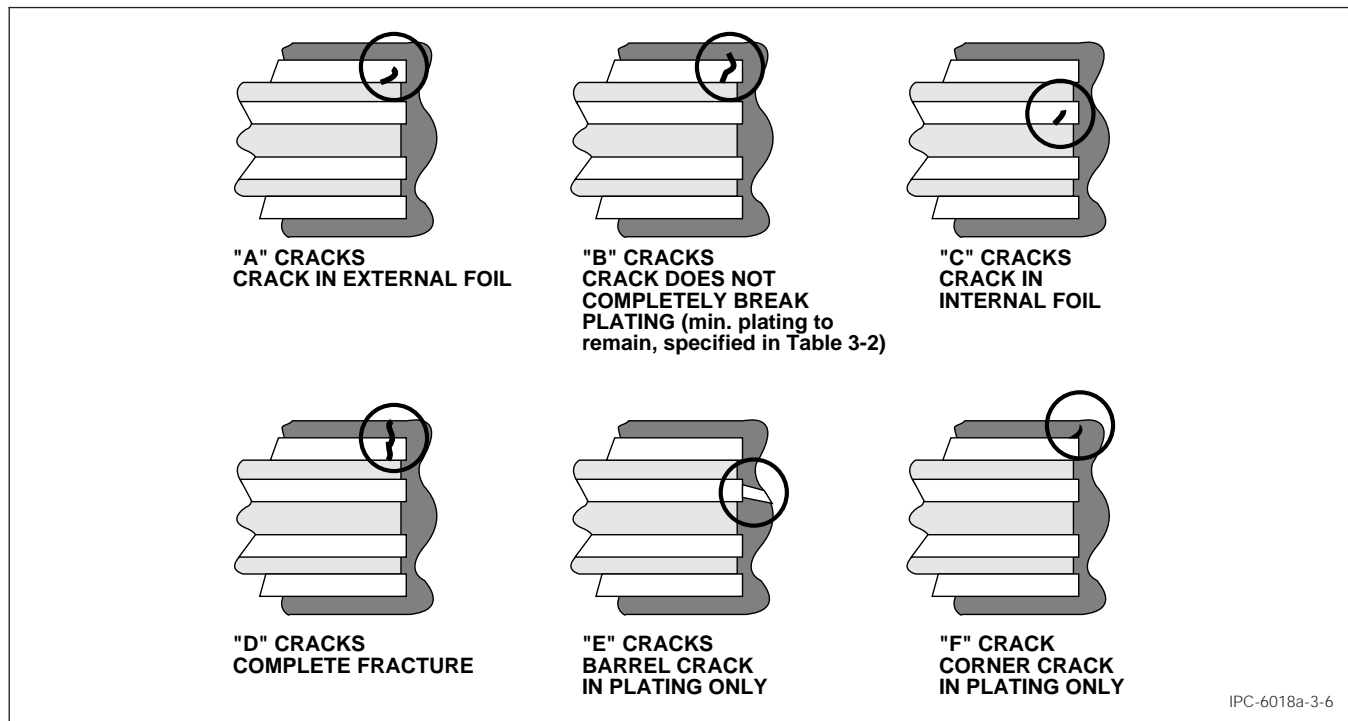


Figure 3-6 Crack Definition

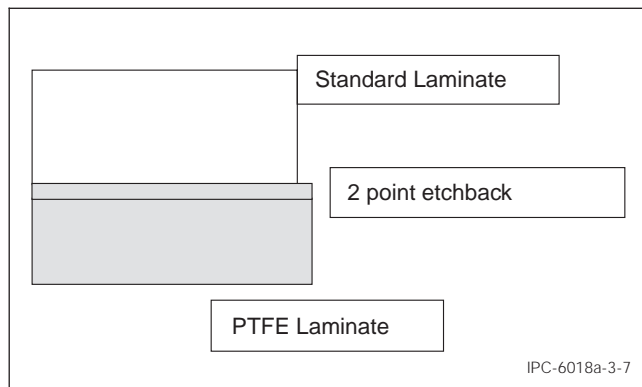


Figure 3-7 Etchback in Contact with PTFE Layer

taken from the affected area and analyzed on the suspect layer(s). Requirements are shown in Table 3-5. Measurement **shall** be as shown in Figure 3-2.

3.7.2.9 Lifted Lands Lifted lands are allowed on the thermally stressed microsection.

3.7.2.10 Plating/Coating Thickness Based on microsection examination, plating/coating thicknesses **shall** meet the requirements of Table 3-2, or as specified in the procurement document. Measurements in the plated-through hole **shall** be reported as an average thickness per side of the hole. Isolated thick or thin sections **shall not** be used for averaging. Isolated areas of reduced copper thickness due to glass fiber protrusions **shall** meet the minimum thickness requirements of Table 3-2 as measured from the end of the protrusion to the hole wall.

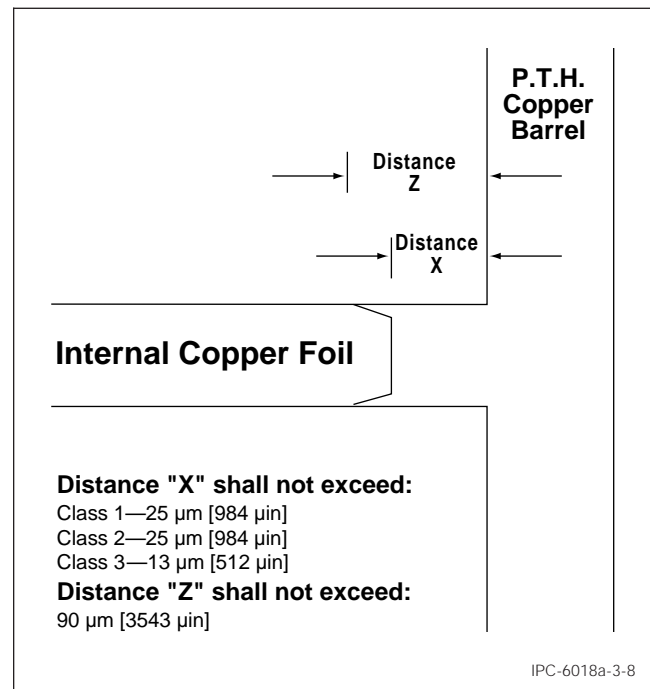


Figure 3-8 Negative Etchback

If copper thickness less than the minimum specified in Table 3-2 is detected in isolated areas, it should be considered a void and resample in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no isolated areas of reduced copper thickness, the product which the test coupons or production boards

represent are considered acceptable; however, if reduced copper thickness is present in the microsections, the product **shall** be considered nonconforming.

3.7.2.11 Minimum Internal Layer Copper Foil Thickness If the internal conductor thickness is specified by a foil weight, the minimum internal copper thickness after processing **shall** be in accordance with Table 3-12 for all classes. When the procurement documentation specifies a minimum copper thickness for internal conductors, the conductor **shall** meet or exceed that minimum thickness.

Table 3-12 Internal Layer Foil Thickness After Processing

Copper Foil			Minimum
Designator	Weight	Starting Thickness	
E	1/8 oz	5 µm [197 µin]	3.5 µm [138 µin]
Q	1/4 oz	9 µm [354 µin]	6 µm [236 µin]
T	3/8 oz	12 µm [472 µin]	8 µm [315 µin]
H	1/2 oz	17 µm [669 µin]	12 µm [472 µin]
1	1 oz	35 µm [1378 µin]	25 µm [984 µin]
2	2 oz	70 µm [2756 µin]	56 µm [2205 µin]
3	3 oz	105 µm [4134 µin]	91 µm [3583 µin]
4	4 oz	140 µm [5512 µin]	122 µm [4803 µin]
Above 4 oz			13 µm [512 µin] below minimum thickness listed for that foil thickness in IPC-4562

3.7.2.12 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-13. When the procurement documentation specifies a minimum copper thickness for external conductors, the test coupon or production board **shall** meet or exceed that minimum thickness.

3.7.2.13 Metal Cores The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or plated-through holes, and the metal plane **shall** be 100 µm [3937 µin] (see Figure 3-9). Test coupons or production boards **shall** have been subjected to thermal stress in accordance with 3.7.1 prior to microsectioning. Wicking, radial cracks, lateral spacing or voids in the hole-fill insulation material **shall not** reduce the electrical spacing between adjacent conductive surfaces to less than 100 µm

Table 3-13 External Conductor Thickness After Plating

Designator	Weight	Base Copper Foil	
		Starting Thickness	Minimum
E	1/8 oz	5 µm [197 µin]	20 µm [787 µin]
Q	1/4 oz	9 µm [354 µin]	22 µm [866 µin]
T	3/8 oz	12 µm [472 µin]	25 µm [984 µin]
H	1/2 oz	17 µm [669 µin]	33 µm [130 µin]
1	1 oz	35 µm [1378 µin]	46 µm [181 µin]
2	2 oz	70 µm [2756 µin]	76 µm [2992 µin]
3	3 oz	105 µm [4134 µin]	107 µm [4213 µin]
4	4 oz	140 µm [5512 µin]	137 µm [5394 µin]
For each succeeding ounce of copper foil, increase minimum conductor thickness by 30 µm [1181 µin]			

[3937 µin]. Wicking and/or radial cracks **shall not** exceed 75 µm [295 µin] from the plated-through hole edge into the hole-fill.

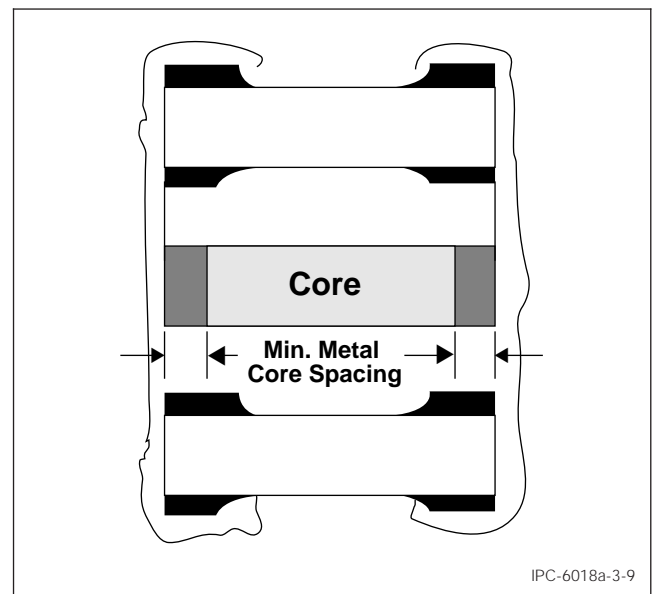


Figure 3-9 Metal Core to Plated-Through Hole Spacing

3.7.2.14 Dielectric Thickness The minimum dielectric spacing **shall** be specified in the procurement documentation.

Note: Minimum dielectric spacing may be specified to be 30 µm [1181 µin]; however, low profile copper foils should be used and the voltages employed should be taken into consideration so as not to cause breakdown between layers. If the minimum dielectric spacing and the number of reinforcing layers are not specified, the minimum dielectric

spacing is 90 μm [3543 μin] and the number of reinforcing layers may be selected by the supplier.

3.7.2.15 Resin Fill of Blind and Buried Vias There is no fill requirement for blind vias. Buried vias **shall** be at least 60% filled with the laminating resin for Class 2 and Class 3. They may be completely void of resin for Class 1.

3.7.2.16 Nailheading No evidence exists that nailheading affects functionality. The presence of nailheading may be considered an indicator of process or design variation but is not a cause for rejection.

3.7.2.17 Lap Shear When specified, lap shear (bond strength) **shall** meet or exceed the requirements as defined on the master drawing. Unless otherwise specified lap shear samples **shall** exhibit a cohesive failure and not an adhesive failure.

Lap shear (bond strength) **shall** be tested at 25°C, \pm 5°C [77°F, \pm 41°F]. In accordance with ASTM-D-3165, the sample **shall** be 25 mm [0.984 in] wide with a 13 mm [0.512 in] lap overlay.

3.8 Other Tests

3.8.1 Metal Core (Horizontal Microsection) All metal core printed boards **shall** meet the requirements of IPC-6012.

3.8.2 Rework Simulation

3.8.2.1 Through-Hole Components When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.4.36, and then microsectioned and examined in accordance with 3.7. Lifted lands are allowed.

3.8.2.2 Surface Mount Components When specified, 100% surface mount boards **shall** be tested in accordance with the procurement documentation.

3.8.3 Bond Strength, Unsupported Component Hole Land The unsupported component hole lands **shall** be tested in accordance with IPC-TM-650, Method 2.4.21. The unsupported component hole land **shall** withstand 2 kg or 500 PSI [3.43 MPa], whichever is less.

Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.9 Solder Resist (Solder Mask) Requirements on Non-PTFE Laminates When solder resist is required on printed boards, it **shall** meet the qualification/conformance requirements of IPC-SM-840. If a solder resist performance class is not specified for Class 1 or 2, IPC-SM-840 Class T **shall** be used. For Class 3 board performance,

IPC-SM-840 Class H **shall** be used. The following other conformance requirements apply:

3.9.1 Solder Resist Coverage Solder resist coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

- a. Metal conductors **shall not** be exposed or bridged by blisters in areas where solder resist is required. Touch up, if required to cover these areas with solder resist, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist.
- b. In areas containing parallel conductors, solder resist variations **shall not** expose adjacent conductors unless the area between the conductors is purposely left blank as for a test point or for some surface mount devices.
- c. Conductors under components **shall not** be exposed or **shall** be otherwise electrically isolated. If the component pattern is not readily apparent, the area covered by a component **shall** be shown in the procurement document.
- d. Solder resist need not be flush with the surface of the land. Misregistration of a solder resist defined feature **shall not** expose adjacent isolated lands or conductors.
- e. Solder resist is allowed on lands for plated-through holes to which solder connections are to be made provided the external annular ring requirements for that Class of products are not violated; resist **shall not** encroach upon the barrel of this type of plated through hole. Other surfaces such as edge board connector fingers and surface mount lands **shall** be free of solder resist except as specified. Solder resist is allowed in plated through holes and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled. Solder resist may tent or plug via holes and may be required for that purpose. Test points that are intended for assembly testing must be free of solder resist unless coverage is specified.
- f. When a land contains no plated-through holes, as in the case of surface mount or ball grid array lands, misregistration **shall not** cause encroachment of the solder resist on the land or lack of solder-resist-definition in excess of the following:
 1. on surface mount lands misregistration **shall not** cause encroachment of the solder resist over the land area greater than 50 μm [1969 μin] for a pitch of 1.25 mm [0.04921 in] or greater; and encroachment **shall not** exceed 25 μm [984 μin] for a pitch less than 1.25 mm [0.04921 in]; encroachment may occur on adjacent sides but not on opposite sides of a surface mount land.

- 2. on ball grid array lands, if the land is solder-resist-defined, misregistration may allow a 90° breakout of the solder resist on the land; if clearance is specified, no encroachment of the solder resist on the land is allowed except at the conductor attachment.
- g. Pits and voids are allowed in nonconductor areas provided they have adherent edges and do not exhibit lifting or blistering in excess of allowance in 3.9.2.
- h. Coverage between closely spaced surface mount lands **shall** be as required by procurement documentation.
- i. When design requires coverage to the board edge, chipping or lifting of solder resist along the board edge after fabrication **shall not** penetrate more than 1.25 mm [0.04921 in] or 50% of the distance to the closest conductor, whichever is less.

3.9.2 Solder Resist Cure and Adhesion The cured solder resist coating **shall not** exhibit tackiness, delamination, or blistering to the following extent:

- Class 1 does not bridge between conductors.
- Class 2 and 3 two per side, maximum size 0.25 mm [0.00984 in] in longest dimension, does not reduce electrical spacing between conductors by more than 25%.

When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured solder resist lifting from the G coupon (see 12.4.6 of IPC-2221) **shall** be in accordance with Table 3-14.

Table 3-14 Solder Resist Adhesion

Surface	Maximum Percentage Loss Allowed		
	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10

3.9.3 Solder Resist Thickness Solder resist thickness is not measured unless specified in the procurement documents. If a thickness measurement is required, instrumental methods may be used or assessment may be made using a microsection of the parallel conductors on the E coupon.

3.10 Circuitry Electrical Continuity and Insulation Resistance Boards **shall** be tested in accordance with IPC-9252.

3.10.1 Circuitry Continuity (Qualification) When required on stripline boards, there **shall** be no open circuits and no circuits **shall** have a resistance greater than that specified on the master drawing.

3.10.2 Circuitry Continuity (Production) Printed boards and qualification test boards **shall** be tested in accordance with the procedure outlined below. There **shall** be no circuits whose resistance exceeds the values established in IPC-9252. Specialized circuitry consisting of long runs of very narrow conductors, or short runs of very large conductors may increase or decrease these values. The acceptability criteria for these specialized conductors must be specified in the procurement documentation.

A current **shall** be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors **shall not** exceed that specified in IPC-2221 for the smallest conductor in the circuit. For qualification, the test current **shall not** exceed one ampere. Boards with designed resistive patterns **shall** meet the resistance requirements specified on the master drawing.

3.10.3 Circuit Shorts The resistance between mutually isolated conductors **shall** be as follows for Class 1, 2 and 3.

- Class 1 — Greater than 2 megohms
- Class 2 — Greater than 15 megohms
- Class 3 — Greater than 100 megohms

A test voltage **shall** be applied between all common portions of each conductor pattern and all adjacent common portions. The voltage **shall** be applied between conductor patterns of each layer and the electrical-isolated pattern of each layer. The minimum applied test voltage **shall** be as specified on the drawing. If the voltage is not specified, the test voltage **shall** be 40 V.

3.10.4 Dielectric Withstanding Voltage Applicable test coupons or production boards **shall** meet the requirements of Table 3-15, without flashover, or breakdown between conductors, or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

Table 3-15 Dielectric Withstanding Voltages

	Class 1	Class 2 and 3
Voltage - For spacing 80 µm [3150 µin] or greater	No requirement	500 Vdc +15, -0
Voltage - For spacing less than 80 µm [3150 µin]	No requirement	250 Vdc +15, -0
Time	No requirement	30 sec +3, -0

3.10.5 Insulation Resistance Printed Boards or qualification test boards **shall** be tested in accordance with the following procedure. The insulation resistance between conductors **shall** meet the values established in IPC-9252.

The voltage applied between networks must be high enough to provide sufficient current resolution for the measurement. At the same time, it must be low enough to prevent arc-over between adjacent networks, which could induce defects within the product. For manual testing, the voltage **shall** be 200 volts minimum and **shall** be applied for a minimum of five seconds. When automated test equipment is used, the minimum applied test voltage **shall** be twice the maximum rated voltage of the board. If the maximum is not specified, the test voltage **shall** be 40 volts minimum.

3.10.6 Circuit/Plated-Through Shorts to Metal Substrate Printed boards **shall** be tested in accordance with 3.10.4 except that polarizing voltage of 500 volts (DC) **shall** be applied between conductors and/or lands and the metallic heatsink in a manner such that each conductor/land area is tested (e.g., using a metallic brush or aluminum foil).

The board **shall** be capable of withstanding 500 volts (DC) between circuitry/plated-through holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

3.10.7 Moisture and Insulation Resistance (MIR) Test coupons **shall** be tested in accordance with the procedure outlined below. The test coupon **shall not** exhibit subsurface imperfections in excess of that allowed in 3.4.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-16 (at 500 volts DC). Noncomponent flush boards **shall** have a minimum requirement of 50 M Ω for all classes. Insulation resistance requirements in the as-received condition are detailed in special requirement section (see 3.12.9).

The moisture and insulation resistance for printed boards **shall** be performed in accordance with IPC-TM-650, Method 2.6.3. Conformal coating in accordance with IPC-CC-830 **shall** be applied to the external conductors prior to chamber exposure. Final measurements **shall** be made at room temperature within two hours after removal from the test chamber. All layers have a 100 ± 10 volts DC polarizing voltage applied during chamber exposure. Measling of the conformal coating **shall not** extend more than 3 mm [0.120 in] from the edge of the test coupon or production board.

3.10.8 Dielectric Withstanding Voltage After MIR A dielectric withstanding voltage test **shall** be performed after moisture and insulation resistance in accordance with 3.10.4.

Table 3-16 Insulation Resistance

	Class 1	Class 2	Class 3
As received	Maintain electrical function	500 M Ω	500 M Ω
After exposure to moisture	Maintain electrical function	100 M Ω	500 M Ω

3.11 Cleanliness Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.3.25, paragraph 4.0, Resistance of Solvent Extract Method. Equivalent methods may be used in lieu of the method specified; however it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified.

3.11.1 Cleanliness Prior to Solder Resist Application When a printed board requires a permanent solder resist coating, the uncoated boards **shall** be within the allowable limits of ionic and other contaminants prior to the application of solder resist coating.

When noncoated printed boards are tested per 3.11, the contamination level **shall not** be greater than an equivalent of 1.56 $\mu\text{g}/\text{cm}^2$ of sodium chloride.

3.11.2 Cleanliness After Solder Resist, Solder, or Alternative Surface Coating Application When specified, printed boards **shall** be tested per 3.11 and meet the requirements in the procurement documentation.

3.11.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination When specified, inner layers **shall** be tested per 3.11 and meet the requirements of the procurement documentation.

3.12 Special Requirements When specified in the procurement documentation, some or all of the special requirements listed in this section (3.12) **shall** apply. A notation in the procurement documentation will designate which are required.

3.12.1 Outgassing Printed boards **shall** be tested in accordance with the procedure outlined below. The degree of outgassing **shall not** result in a total mass loss of more than 0.1%.

Mass loss **shall** be determined on test coupons or production boards of representative substrates when tested per IPC-TM-650, Method 2.6.4. Test substrates **shall** be approximately 1 cm^3 in volume. The substrates **shall** be placed in a vacuum chamber capable of achieving 7×10^{-3} Pa [5×10^{-5} mm Hg or torr] for 24 hours.

3.12.2 Organic Contamination Noncoated printed boards **shall** be tested in accordance with the procedure outlined below. Any positive identification of organic contamination **shall** constitute a failure.

The printed board **shall** be tested in accordance with IPC-TM-650, Methods 2.3.38 or 2.3.39. The first is a qualitative method in which very pure acetonitrile is dripped across the test coupon or production board and collected on a microscope slide. It is dried and compared with a slide having dried, uncontaminated acetonitrile on it for visual evidence of organic residue. If evidence of organic contamination is detected by this test, Method 2.3.39 is used to determine the nature of the contaminant by the use of infrared spectrophotometric analysis using the Multiple Internal Reflectance (MIR) method.

3.12.3 Fungus Resistance Completed boards or representative board sections from the lot **shall not** support fungus growth when tested as follows: The specimen(s) **shall** be tested in accordance with IPC-TM-650, Method 2.6.1.

3.12.4 Vibration The test coupon or production board **shall** pass the circuitry test in 3.10.2 following the vibration test procedure below and **shall not** exhibit bow or twist in excess of that allowed in 3.5.4 following testing.

The boards **shall** be subjected to both a cycling and resonance dwell test with the flat surface of the board mounted perpendicular to the axis of vibration in accordance with IPC-TM-650, Method 2.6.9.

Cycling test — The cycling test **shall** consist of one sweep from 20 to 2000 Hz performed in 16 minutes. Input acceleration over the 20 to 2000 Hz frequency range **shall** be maintained to 15 Gs.

Resonance dwell — Test coupons or production boards **shall** be subjected to a 30 minute resonance dwell with 25 Gs input or a maximum of 100 Gs output measured at the geometric center of the test coupon or production board. The test coupons or production boards **shall** be restrained from movement by fixturing on all four sides.

3.12.5 Mechanical Shock The test boards **shall** pass the circuitry test in 3.10.2 after being subjected to mechanical shock testing as follows.

The mechanical shock test **shall** be performed in accordance with IPC-TM-650, Method 2.6.5. The boards **shall** be subjected three times to a shock pulse of 100 Gs with a duration of 6.5 milliseconds in each of the three principal planes. The test coupons or production boards **shall** be restrained from movement by fixturing on all four edges.

3.12.6 Impedance Testing Requirements for impedance **shall** be specified on the master drawing. Impedance testing may be performed on a test coupon or a designated circuit in the production board. Ensure that the connection points on the coupon suit the impedance test probe footprint. Time Domain Reflectometers (TDR) are used for electrical testing, but for large impedance tolerances,

mechanical measurements from a microsection utilizing a special test coupon can be used to calculate and verify impedance values. (See IPC-2141 for the equations for calculating impedance from the test coupon and IPC-TM-650, Method 2.5.5.7 for the test method using the TDR technique.)

3.12.7 Coefficient of Thermal Expansion (CTE) When boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the Coefficient of Thermal Expansion **shall** be within ± 2 ppm/°C for the CTE and temperature range specified on the procurement documentation. Testing **shall** be by the strain gauge method in accordance with IPC-TM-650, Method 2.4.41.2. If agreed upon by user and supplier, other methods of determining the CTE may be used.

3.12.8 Thermal Shock When specified, printed boards or test coupons **shall** be tested for 100 cycles from -65°C to +105°C [-85°F to 221°F], in accordance with IPC-TM-650, Method 2.6.7.2. An increase of 10% or more **shall** be considered a reject. After microsectioning, the boards or test coupons **shall** meet the requirements of Table 3-11 and Figure 3-6.

For polytetrafluoroethylene (PTFE) material types, the board or test coupon **shall** meet the circuitry requirements of 3.10.2 at room temperature after the 100th cycle and no microsectioning is required.

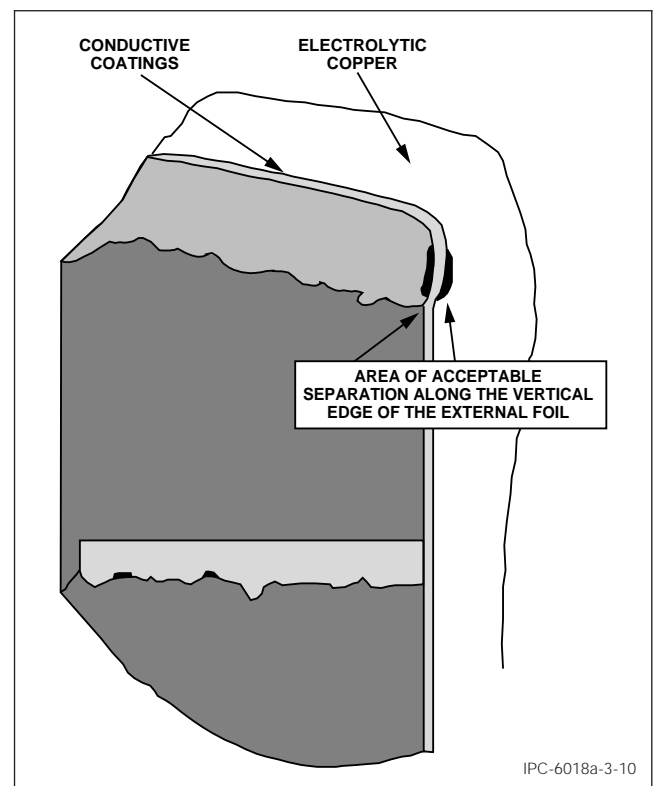


Figure 3-10 Separations at External Foil

3.12.9 Surface Insulation Resistance (As Received)

Test coupons **shall** be tested in accordance with the procedure outlined below. The insulation resistance **shall** be no less than that shown in Table 3-16.

Test coupons or production boards should be conditioned at $50^{\circ}\text{C} \pm 5^{\circ}\text{C}$ [$122^{\circ}\text{F} \pm 41^{\circ}\text{F}$] with no added humidity for a period of 24 hours. After cooling, the insulation resistance test **shall** be performed in accordance with the ambient temperature measurements specified in IPC-TM-650, Method 2.6.3.

3.12.10 Wire Bond Adhesion Requirements for wire bond adhesion **shall** be specified on the procurement documentation. IPC-6015 specifies acceptance criteria and test methods for wire bond adhesion on MCM-Ls.

3.12.11 Die Bond Adhesion Requirements for die bond adhesion **shall** be specified on the procurement documentation. IPC-6015 specifies acceptance criteria and test methods for die bond adhesion on MCM-Ls.

3.13 Repair Repair of bare boards **shall** be as agreed upon between the user and supplier (see IPC-7721).

3.13.1 Circuit Repairs When agreed on between user and supplier, circuit repairs on Classes 1, 2, and 3 will be permitted. As a guideline, there should be no more than two circuit repairs for each 0.09 m^2 or less of layer area per side. Circuit repairs on any impedance controlled circuits **shall not** violate the impedance requirement and **shall** have the agreement of the user. Circuit repairs **shall not** violate the minimum electrical spacing requirements.

3.14 Rework Rework is permitted for all Classes. The touch-up of surface imperfections in the base material or removal of residual plating materials or extraneous copper will be permitted for all products when such action does not affect the functional integrity of the board.

4 QUALITY ASSURANCE PROVISIONS

4.1 General General Quality Assurance Provisions are specified in IPC-6011 and each sectional specification. The requirements specific for High Speed/High Frequency Boards are contained in this specification and include the Qualification Testing, Acceptance Testing and Frequency Quality Conformance Testing.

4.1.1 Qualification Qualification is agreed upon by the user and supplier (see IPC-6011). The qualification should consist of preproduction samples, production sample or test coupons (see IPC-6011) that are produced by the same equipment and procedures planned for the production boards. Qualification as agreed by the user may consist of documentation that supplier has furnished similar product

to other users or to other similar specifications. A production board may be used for Qualification as long as the board type is agreed upon between Supplier and Customer.

4.1.2 Sample Test Coupons Sample test coupons may be used for qualification or for on-going process control. Master drawings, databases, or phototools are available from IPC. For board Types 4-7 end product **shall** have modifications to the IPC Master Drawing IPC-100103 within IPC-A-47 to include blind and buried vias. (See 1.4)

4.2 Acceptance Tests Use the C=0 Sampling Plan specified in Table 4-2 when "Sample" is indicated in Table 4-3. Acceptance testing **shall** be performed as specified in Table 4-3 to the requirements of this specification and IPC-6011 using either test coupons and/or production boards. The test coupons referenced are described in IPC-2221 and indicate purpose of coupon and its frequency on a manufacturing panel. IPC provides the artwork for these test coupons within the IPC-A-47 Composite Test Pattern Ten Layer Phototool.

4.2.1 C=0 Sampling Plan The C=0 Sampling Plan provides greater or equal protection for the Lot Tolerance Percent Defective (L.T.P.D.) protection at the 0.010 "consumer risk" level. The Index Values at the top of each sample size column associates to the A.Q.L. level. For a lot to be accepted, all samples (shown in Table 4-2) **shall** conform to the requirements. Any review and disposition of a rejected lot shall be fully documented. Contact the American Society for Quality Control for more information on sampling plans (Zero Acceptance Number Sampling Plans - H0862).

4.2.2 Referee Tests Two additional microsection sets from the same panel may be prepared and evaluated for microsection defects that are considered to be isolated or random in nature or caused by microsection preparation. Referee tests shall be documented and have customer participation. For acceptance, both referee sets must be defect free.

4.3 Quality Conformance Testing Quality Conformance Testing shall consist of inspections specified in Table 4-4 in a laboratory which meets all requirements of IPC-QL-653, unless otherwise specified by the user. Class 3 testing may be extended to reliability test and evaluation for Class 2.

4.3.1 Coupon Selection Two sets of test coupons of the most complex pattern of each type of material processed during the inspection period **shall** be selected from lots that have passed acceptance testing.

4.3.2 Test Equipment and Inspection Facilities Test and measuring equipment and inspection facilities of sufficient accuracy, quality, and quantity to permit performance

of the required inspection **shall** be established and maintained by the supplier. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment **shall** be in accordance with an alternative statistically sound calibration procedure.

4.3.3 Tolerances Unless otherwise specified, all laboratory equipment/conditions shall have tolerances of $\pm 5\%$.

Table 4-1 specifies the test coupons on the sample used for qualification and process capability evaluations.

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,4,7	Types 5,6	Board
Visual (1)	All	All	All	X
Solderability Surface (1) Hole (1)	M2,M5	S1,S6	S1,S6	
Dimensional (1)	All	All	All	X
Physical Plating Adhesion (1) Bond Strength	N1,N4,N5 A2,A3,A6	N1,N4,N5 A2,A3,A6	N1,N4,N5 A1,A3,A6	
Construction Integrity PTH Prior to Stress Additional Dimensions		A1,A4,A5 A1,A4,A5	Design Req. Design Req.	
PTH After Stress Thermal Stress Horizontal micro (Metal Core) Rework Simulation		B1,B4,B5 A1,B4,B5 B2,B3,B6	Design Req. A1,B4,B5 Design Req.	
Electrical Requirements DWV Continuity Insulation Resistance	E1,E4,E5 D1,D4,D5 E2,E3,E6	E1,E4,E5 D1,D4,D5 E2,E3,E6	E1,E4,E5 Design Req. E2,E3,E6	
Environmental Thermal Shock Cleanliness (1)	D2,D3,D6	D2,D3,D6	Design Req.	X
Special Requirements(2) Outgassing Organic Contamination Fungus Vibration Mechanical Shock Impedance Thermal Expansion		H1,H2,H3		X X X X

Note 1 - Not technology dependent.

Note 2 - Additional test coupons required, to be agreed upon between user and manufacturer.

Table 4-2 C=0 Sampling Plan (Sample Size for Specific Index Value*)

Lot Size	Class 1			Class 2			Class 3			
	2.5*	4.0*	6.5*	1.5*	2.5*	4.0*	0.10*	1.0*	2.5*	4.0*
1-8	5	3	2	**	5	3	**	**	5	3
9-15	5	3	2	8	5	3	**	13	5	3
16-25	5	3	3	8	5	3	**	13	5	3
26-50	5	5	5	8	5	5	**	13	5	5
51-90	7	6	5	8	7	6	**	13	7	6
91-150	11	7	6	12	11	7	125	13	11	7
151-280	13	10	7	19	13	10	125	20	13	10
281-500	16	11	9	21	16	11	125	29	16	11
501-1200	19	15	11	27	19	15	125	34	19	15
1201-3200	23	18	13	35	23	18	125	42	23	18
3201-10,000	29	22	15	38	29	22	192	50	29	22
10,001-35,000	35	29	15	46	35	29	294	60	35	29

* Index Value is associated to the A.Q.L. value. If a particular product is determined to be "critical" by the user and a smaller index value is required, the user **shall** designate the requirement in the procurement document and should state the "critical" requirement on the master drawing.

** Denotes inspect entire lot.

Table 4-3 Acceptance Testing and Frequency

Inspection	Requirement and Method Section	Sample		Test Frequency			Remarks
		Production Board	Test Coupon by Board	Class 1 ¹	Class 2 ¹	Class 3 ¹	
Material	3.3.1 - 3.3.12			Manufacturer's Certification			Verifiable certificate of compliance or SPC program
Visual							
Edges of board	3.4.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Laminate imperfections	3.4.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Voids in plated holes and coatings	3.4.3	X		Sample (4.0)	Sample (2.5)	Sample (1.0)	Per panel
Lifted lands	3.4.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Marking and traceability	3.4.5	X	Coupons and board	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Workmanship	3.4.9	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solderability							
Surface/Hole	3.4.6		C and A	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Dimensional							
Board dimensional	3.5	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Hole pattern accuracy	3.5.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Minimum 10 evaluations per board
Annular ring and breakout (internal)	3.5.2		A/B or F	Not required	Sample (1.5) Type 3-6 only	Sample (1.0) Type 3-6 only	Per panel (4 coupons)
Annular ring (external)	3.5.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Bow & twist	3.5.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solder resist coverage	3.9 - 3.9.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Plating/coating thickness	3.7.2.10	X	C	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Conductor Width	3.6.2 3.6.2.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel layer
Conductor Definition	3.6	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel layer
Conductor Spacing	3.6.2 3.6.2.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel layer (minimum 5 per layer set)
Conductive Surfaces (Surface Only)							
Edge board contact, junction of gold plate to solder finish	3.4.8	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Conductive Surface Nicks, dents, pinholes	3.6.3.1 - 3.6.3.5	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board

Inspection	Requirement and Method Section	Sample		Test Frequency						Remarks
		Production Board	Test Coupon by Board	Class 1 ¹		Class 2 ¹		Class 3 ¹		
Dewetting/ nonwetting	3.6.3.8 3.6.3.9	X		Sample (6.5)		Sample (4.0)		Sample (2.5)		Per board
Edge board connector	3.6.3.7	X		Sample (6.5)		Sample (4.0)		Sample (2.5)		Per board
Surface mount	3.6.3.6	X		Sample (6.5)		Sample (4.0)		Sample (2.5)		Minimum 10 evaluations per panel
Physical										
Plating adhesion	3.4.7	X	C	Sample (6.5)		Sample (4.0)		Sample (4.0)		Per panel (1 coupon)
Solder resist cure & adhesion	3.9.2		G	Sample (6.5)		Sample (4.0)		Sample (4.0)		Per panel (1 coupon)
Structural Integrity After Stress Types 3-6 (Microsection)										
Plating integrity	3.7.2.1		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Laminate integrity	3.7.2.3		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Etchback/ negative etchback	3.7.2.5.1 - 3.7.2.7		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Annular ring (internal)	3.7.2.8		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Lifted lands	3.7.2.9		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Hole plating thickness	3.7.2.10		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Surface plating and conductor thickness	3.7.2.10 - 3.7.2.12		A,B,or C	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Conductor thickness (internal)	3.7.2.11		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Metal core spacing	3.7.2.13		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Dielectric thickness	3.7.2.14		A or B	Sample (2.5)		Sample (1.5)		Sample (0.1)		Per panel (1 coupon)
Resin fill of blind/buried vias	3.7.2.15		A or B	Sample (6.5)		Sample (4.0)		Sample (4.0)		Per panel structural integrity after stress type 2 (microsection)
Structural Integrity After Stress Type 2 (Microsection)										
Plating integrity	3.7.2.1		A or B	Sample (6.5)		Sample (4.0)		Sample (2.5)		Per panel
Laminate integrity	3.7.2.3		A or B	Sample (6.5)		Sample (4.0)		Sample (2.5)		Per panel
Lifted lands	3.7.2.9		A or B	Sample (6.5)		Sample (4.0)		Sample (2.5)		Per panel
Hole Plating thickness	3.7.2.10		A or B	Sample (6.5)		Sample (4.0)		Sample (2.5)		Per panel
Surface plating and conductor thickness	3.7.2.10 - 3.7.2.12		A or B	Sample (6.5)		Sample (4.0)		Sample (2.5)		Per panel
Electrical										
Circuit continuity	3.10 - 3.10.3	X		Type 1-2 ²	Type 3-6 Sample (2.5)	Type 1-2 ²	Type 3-6 100%	Type 1-2 ²	Type 3-6 100%	Per board

Inspection	Requirement and Method Section	Sample		Test Frequency						Remarks
		Production Board	Test Coupon by Board	Class 1 ¹		Class 2 ¹		Class 3 ¹		
Insulation resistance	3.10.5	X		Type 1-2 ²	Type 3-6 Sample (2.5)	Type 1-2 ²	Type 3-6 100%	Type 1-2 ²	Type 3-6 100%	Per board
Cleanliness										
Cleanliness prior to solder resist application	3.11.1									
Special Requirements (when specified)										
Metal core (horizontal microsection)	3.8.1									
Solder resist thickness	3.9.3									
Dielectric withstanding voltage	3.10.4									
Circuit/plated-through shorts to metal substrate	3.10.6									
Cleanliness after surface coating application	3.11.2									
Cleanliness of inner layers after oxide treatment prior to lamination	3.11.3									
Outgassing	3.12.1									
Organic contamination	3.12.2									
Fungus resistance	3.12.3									As specified by contract or master drawing
Vibration	3.12.4									
Mechanical shock	3.12.5									
Impedance testing	3.12.6									
Coefficient of thermal expansion	3.12.7									
Thermal shock	3.12.8									
Surface insulation resistance (as received)	3.12.9									
Wire Bond Adhesion	3.12.10									
Die Bond adhesion	3.12.11									
Repair	3.13									
Circuit repair	3.13.1									

Note

1. Number in parentheses is the AQL level
2. For Type 1 and 2 boards, visual or AOI inspection may be used in lieu of electrical testing.

Table 4-4 Quality Conformance Testing

Inspection	Requirement and Method Section	Test Coupon		Test Frequency		
		Type 1	Type 2-6	Class 1	Class 2	Class 3
Rework simulation (when specified)	3.8.2	—	A or B ¹	NA	NA	Monthly
Bond strength	3.8.3	B	—	NA	Quarterly	Monthly
Dielectric withstanding voltage	3.10.4	E	E	NA	Quarterly	Monthly
Moisture and insulation resistance	3.10.7	E	E	NA	Quarterly	Monthly

¹Test Coupon B contains the largest component hole and land associated with that hole that can be fitted on a 2.5 mm [0.0984 in] grid.

5 PACKAGING

Unless otherwise specified, each printed board **shall** be individually unit-packaged. Printed boards **shall** be clean, dry, and packaged in a manner that will afford adequate protection against corrosion, deterioration, and physical damage during shipment from supply source to the customer.

If the finished board to be packaged has a thickness of 0.050 mm [0.00197 in] or less, the individually packaged boards **shall** be placed into a larger water—vapor proof outer bag. This outer bag **shall** also contain a stiffener(s) of the same size or larger than the profile of the board being shipped and **shall** have a thickness of 1.00 mm [0.03937 in] or greater. The stiffener may be fabricated from acrylic, phenolic or laminate (FR4, etc.) material with the copper removed.

6 NOTES

6.1 Ordering Data Procurement documents should specify the following:

- A. Title, number, and date of this specification.
- B. Specific exceptions from this specification, if any.

- C. Title, number, and date of the applicable master drawing.
- D. Part identification and marking instructions.
- E. Information for preparation of delivery, if applicable.
- F. Acceptance level classifications and inspection requirements.
- G. Other
- H. Master Drawing to include:
 1. Material type
 2. Marking
 3. Workmanship
 4. Plating type
 5. Conductor pattern and edges
 6. Conductor pattern width
 7. Conductor gap
 8. Registration
 9. Lap shear
 10. Critical pattern areas requiring special attention
 11. Test data as required

APPENDIX A

The following provides information on selection of samples from production lots, and details the methods that may be used for establishing various anomaly criteria.

Below is an example of the hypothetical inspection flow which is illustrated by Figure A-1.

1. A Class 3 printed board wiring is to be inspected for five criteria requiring sampling: 4 major and 1 minor.
2. Several production lots make up the total inspection lot of 180.
3. Using Table 12, the largest sample size (major defect) is determined to be 20 samples.
4. The inspector takes 13 samples and inspects for both major and minor defects. The remaining seven samples are inspected for only major defects.

Note: If during the inspection of the final seven samples, a minor defect is discovered it **shall not** be cause for lot rejection but **shall** be noted in the report.

Classification of Requirements

The user has the responsibility to establish the classification of all requirements for the printed board products. In this regard, the user has the opportunity to indicate all requirements that may be of a major or minor or critical nature, or he may provide a check-off list that establishes the mix and match criteria of various examinations.

As an example, visual examinations look for uniformity and appearances, freedom from foreign materials, inclusions, peeling, roughness and discoloration. In addition, scratches, voids and other forms of surface imperfections are also examined as are the requirements for coverage of conductor edges.

Although it is recommended that a single anomaly classification be established for visual requirement, it should be noted that discoloration would normally be considered a cosmetic defect while peeling might be considered a major defect.

Table A-1 provides a check-off list that designates the requirements for military hardware. All requirements have been detailed and have been determined as being critical, major, minor, or cosmetic.

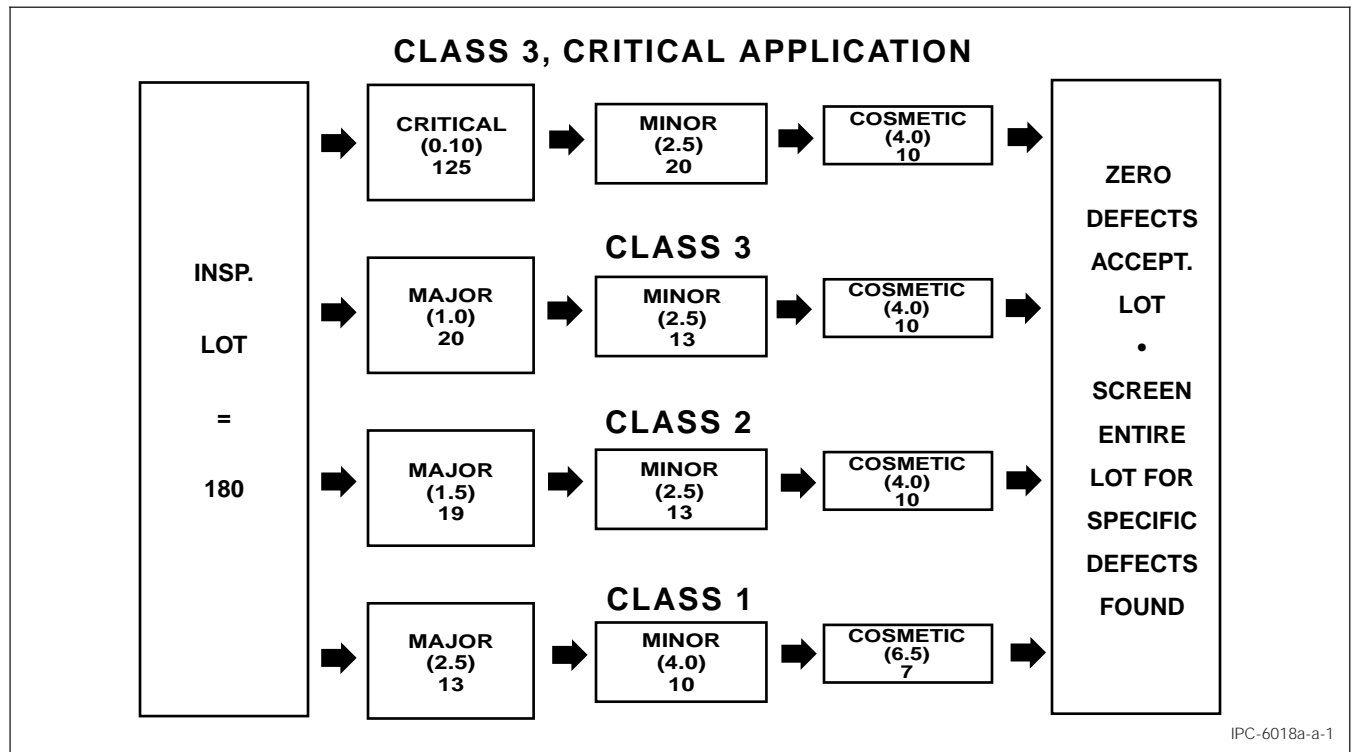


Figure A-1 Zero Defects Graphic Illustration



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ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

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If space not adequate, use reverse side or attach additional sheet(s).

Artwork: Not Applicable Required To be supplied

Included: Electronic File Name: _____

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TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, and job opportunities. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Gencam@ipc.org

Gencam deals with issues regarding the Gencam™ standards and specifications for Printed Circuit Board Layout and Design.

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For more information, contact Keach Sasamori

tel 847/790-5315

fax 847/504-2315

e-mail: sasako@ipc.org

www.ipc.org/html/forum.htm

Education and Training

IPC conducts local educational workshops and national conferences to help you better understand conventional and emerging technologies. Members receive discounts on registration fees. Visit www.ipc.org to see what programs are coming to your area.

IPC Certification Programs

IPC provides world-class training and certification programs based on several widely-used IPC standards, including the IPC-A-610, the J-STD-001, and the IPC-A-600. IPC-sponsored certification gives your company a competitive advantage and your workforce valuable recognition.

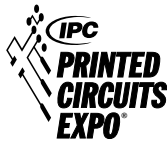
For more information on programs, contact Alexandra Curtis
 tel 847/790-5377 fax 847/509-9798
 e-mail: curtal@ipc.org www.ipc.org

IPC Video Tapes and CD-ROMs

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness. Members receive discounts on purchases.

For more information on IPC Video/CD Training, contact Mark Pritchard
 tel 505/758-7937 ext. 202 fax 505/758-7938
 e-mail: markp@ipcvideo.org www.ipc.org

IPC Printed Circuits Expo[®]



IPC Printed Circuits Expo is the largest trade exhibition in North America devoted to the PWB manufacturing industry. Over 90 technical presentations make up this superior technical conference. Visit www.ipcprintedcircuitexpo.org for upcoming dates and information.

Exhibitor information:

Contact: Mary MacKinnon
 Sales Manager
 tel 847/790-5386
 e-mail: MaryMacKinnon@ipc.org

Registration information:

Alicia Balonek
 Exhibits Manager
 tel 847/790-5398
 e-mail: AliciaBalonek@ipc.org

APEX[®] / IPC SMEMA Council Electronics Assembly Process Exhibition & Conference



APEX is the premier technical conference and exhibition dedicated entirely to the electronics assembly industry. Visit www.GoAPEX.org for upcoming dates and more information.

Exhibitor information:

Contact: Mary MacKinnon
 tel 847/790-5386
 e-mail: MaryMacKinnon@ipc.org

Registration information:

tel 847/790-5360
 fax 847/509-9798
 e-mail: goapex@ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:

Jeanette Ferdman, Membership Director
 tel 847/790-5309 fax 847/509-9798
 e-mail: JeanetteFerdman@ipc.org www.ipc.org

Application for IPC Site Membership



Thank you for your decision to join IPC, Association Connecting Electronics Industries. IPC membership is site specific, which means that benefits of IPC membership are extended only to employees at the site that is designated on this application. To help IPC serve your member site in the most effective manner possible, please tell us what work is being done at your site by choosing the most appropriate member category. *(Check one box only.)*

INDEPENDENT PRINTED CIRCUIT BOARD MANUFACTURER

This facility manufactures, and sells to other companies, printed wiring boards (PWB's) or other electronic interconnection products on the merchant market.

What products do you make for sale?

One- and two-sided rigid, multilayer printed boards Flexible printed boards Other interconnections

Site General Manager _____
Name Title

EMSI COMPANY - Independent Electronics Assembly

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Site General Manager _____
Name Title

OEM - Original Equipment Manufacturer

This facility purchases and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line?

Site General Manager _____
Name Title

INDUSTRY SUPPLIER

This facility supplies raw materials, machinery, equipment, or services used in the manufacture or assembly of electronic interconnection products.

What products or services does your company supply? (50 word limit, please)

The information that you provide here will appear in the next edition of the IPC Membership Directory.

Our company supplies:

GOVERNMENT AGENCY/ACADEMIC TECHNICAL LIAISON

This government agency or accredited university, college or technical training school is directly concerned with design, research and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Application for IPC Site Membership



Site Information: (Please print or type)

Company Name			
Street Address			
City	State	Zip/Postal Code	Country
Main Switchboard Phone No	Main Fax No.		
Company E-Mail Address	Website URL		
Name of Primary Contact for all IPC matters	Title	Mail Stop	
Phone No.	Fax No	E-Mail	
Name of Senior Management Contact:	Title:	Mail Stop	
Phone No	Fax No	E-Mail	

Please attach business card of primary contact here.

Please designate your site's Technical Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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Please designate your site's Management Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail
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Application for IPC Site Membership



MEMBERSHIP DUES SCHEDULE

Please check one:

- \$1,000.00** – Annual dues for Primary Site Membership
Twelve months of IPC membership begins from the time the application and payment are received at the IPC office.
- \$800.00** – Annual dues for Additional Facility Membership
An additional membership for a site within an organization where there already is a current Primary Site IPC membership.
- \$600.00**** – Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than \$1,000,000.00. USD
** Please provide proof of annual sales.
- \$250.00** – Annual dues for Government Agency or Academic Technical Liaison Membership. Must be not-for-profit organization.

TMRC MEMBERSHIP

- Please send information on participation in the Technology Market Research Council (TMRC) program. Only current IPC member sites are eligible to participate in this **calendar year** program, which is available for an additional fee.
- Yes, sign up our site now:**
 - \$950.00** - Primary TMRC member site
 - \$400.00** - Additional facility TMRC member. Another site within our organization is already a TMRC program participant.

Name of Primary Contact for all TMRC matters:

Phone _____ Fax _____

E-Mail _____

PAYMENT INFORMATION

Enclosed is our check/money order for \$ _____

Mail application with check or money order to:

IPC
Dept. 77-3491
Chicago, IL 60678-3491

Fax or mail application with credit card payment to:

IPC
*2215 Sanders Road
Northbrook, IL 60062-6135
Tel: 847-509-9700
Fax: 847-509-9798

** Overnight deliveries to this address only*

Please bill my credit card (circle one) for \$ _____

- MasterCard American Express Visa Diners Club

Account No _____ Expiration Date _____

Name of Card Holder _____

Authorized Signature _____

Phone Number _____

QUESTIONS ?

Call the IPC Member Services Department in Northbrook, Illinois,
at: 847-509-9700 (extensions 5309/5372)
or fax us at 847.509-9798

E-mail: JeanetteFerdman@ipc.org SusanStorck@ipc.org

Application for IPC Site Membership



INFORMATION DISTRIBUTION

IPC has significant member benefits available to a wide range of individuals within your organization. To ensure that your facility takes advantage of these benefits, please provide the name of the individual responsible for each of the functional areas listed below. If one person has multiple responsibilities, please list that person's name as many times as necessary.

Chief Executive:

Name	Title/Mail Stop	Phone	Fax	E-mail
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Sales/Marketing:

Name	Title/Mail Stop	Phone	Fax	E-mail
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Finance (CFO)

Name	Title/Mail Stop	Phone	Fax	E-mail
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Human Resources

Name	Title/Mail Stop	Phone	Fax	E-mail
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Environmental/Safety

Name	Title/Mail Stop	Phone	Fax	E-mail
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Design/Artwork

Name	Title/Mail Stop	Phone	Fax	E-mail
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Product Assurance

Name	Title/Mail Stop	Phone	Fax	E-mail
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Manufacturing

Name	Title/Mail Stop	Phone	Fax	E-mail
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Training

Name	Title/Mail Stop	Phone	Fax	E-mail
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Purchasing

Name	Title/Mail Stop	Phone	Fax	E-mail
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IPC REVIEW SUBSCRIPTION LIST

One of the many benefits of IPC membership is a subscription to the *IPC Review*, our monthly magazine. Please list below the names of individuals who would benefit from receiving our magazine, which provides information about the industry, IPC news, and other items of interest. A subscription for the IPC Primary Contact person is entered automatically.

Name	Title/Mail Stop
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Name	Title/Mail Stop
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Name	Title/Mail Stop
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Name	Title/Mail Stop
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Name	Title/Mail Stop
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Name	Title/Mail Stop
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ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

Standard Improvement Form

IPC-6018A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798
answers@ipc.org

1. I recommend changes to the following:

Requirement, paragraph number _____
 Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

Unclear Too Rigid In Error
 Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name _____ Telephone _____

Company _____ E-mail _____

Address _____

City/State/Zip _____ Date _____



ASSOCIATION CONNECTING
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